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(54) **Video signal transmission system and method and apparatus for coding a video signal.**

(57) In a video signal transmission system, in which video signals are transformed to high efficiency coded data and are then transmitted, a quantization step size is enlarged in quantizing picture data intra coded to be effectively avoided the amount of data generated excessively increasing. The data residual amount of transmission buffer memory is set to a small level as compared to the data residual amount at which the frame dropping is completed. Video signals which are intra coded are then sent immediately after a transmission line is connected to a destination to be enhanced in facility.

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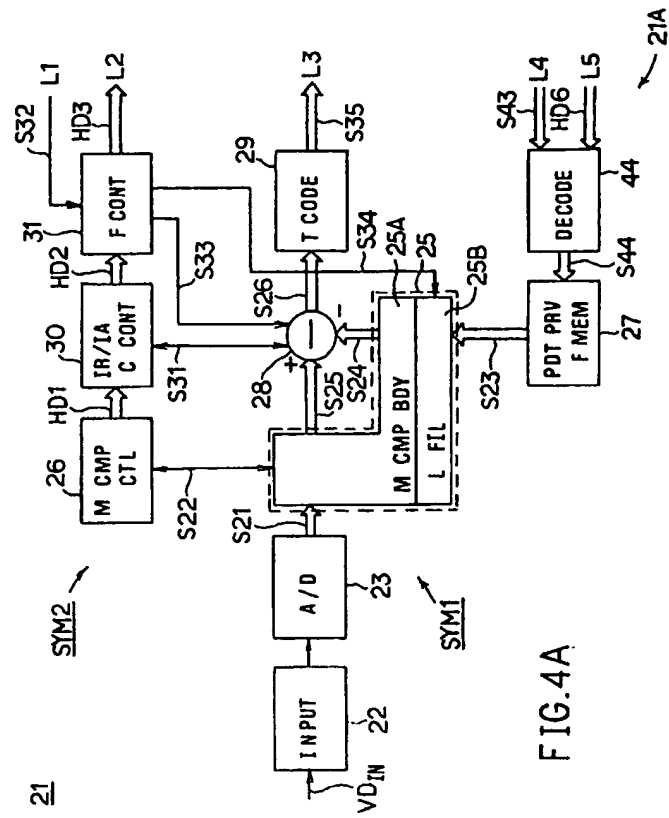


FIG. 4A

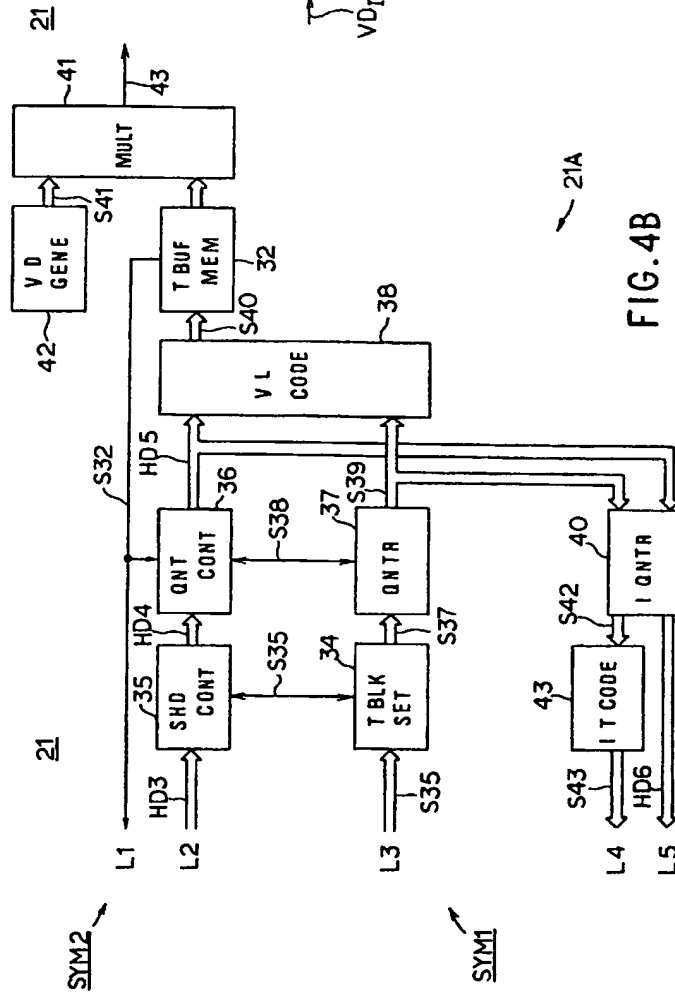


FIG. 4B

VIDEO SIGNAL TRANSMISSION SYSTEM AND METHOD AND APPARATUS FOR CODING VIDEO SIGNAL

This invention relates to a video signal transmission system, and more particularly is suitably applied to a case in which video signals are transformed to high efficiency coded data and are then transmitted, for example.

In the picture phone system and the video conference system, heretofore there has been proposed a video signal transmission system in which video signals which constitute moving pictures are high efficiency coded to provide intra coded frame data and inter coded frame data, and thereby the moving picture video signals are transmitted through transmission lines with relatively strict limits in transmission capacity (Japanese Patent Laid-open Publication No. 63 (1988)-1183).

More specifically, in a case where pictures PC1, PC2, PC3, ... which constitutes moving pictures at respective times $t = t_1, t_2, t_3, \dots$ are transmitted as shown in FIG. 1, the transmission efficiency is enhanced by compressing the picture data to be transmitted, using a fact that video signals are large in autocorrelation according to the lapse of time. In the intra coding, pictures PC1, PC2, PC3, ... are compressed in such a manner that differences are determined by comparing pixel data with a predetermined reference value. Thus, picture data of each picture PC1, PC2, PC3, ... is transmitted at an amount of data compressed using the autocorrelation between pixel data in the same frame.

In the inter coding, picture data PC1, PC2, PC3, ... which are differences between two successive pictures PC1 and PC2, PC2 and PC3, ..., respectively, are determined as shown in FIG. 1, and are transmitted together with the intra coded picture data of the original picture PC1 at the time $t = t_1$.

Thus, it is possible to send the pictures PC1, PC2, PC3, ... in the format of high efficiency coded digital data which is markedly small in amount as compared to data in a case where all the picture data is sent.

The coding of such picture signals is achieved by a picture data generating system 1 having a configuration shown in FIG. 2.

The picture data generating system 1 performs processing operations, such as every other field dropping and every other field line dropping, on input video signals VD in a preprocessing circuit 2. Subsequently, the luminance signals and chrominance signals thereof are transformed to transmission unit block (referred to as macro block) data S11 which is 16 pixels (horizontal) x 16 pixels (vertical) data, and are then fed to a picture data coding circuit 3.

The picture data coding circuit 3 accepts predicted current frame data S12 constructed in a prediction coding circuit 4, and determines the difference between the predicted current frame data S12 and the macro block data S11 to produce inter coded data (this is referred to as inter coding mode) or the difference between the macro block data S11 and the reference data to generate intra coded data. This data is fed to a transform coding circuit 5 as differential data S13.

The transform coding circuit 5 consists of a discrete cosine transform circuit and provides transform coded data S14, high efficiency coded by orthogonal transforming the differential data S13, to a quantizer 6, which sends quantized picture data S15.

The quantized picture data S15 thus obtained from the quantizer 6 is high efficiency coded again in a retransform coding circuit 7 which includes a variable length coding circuit and is then fed as transmission picture data S16 to a transmission buffer memory 8.

Moreover, the quantized picture data S15 undergoes inverse quantization and inverse transform coding operations in the prediction coding circuit 4, so that the quantized picture data S15 is decoded to differential data. Then, the predicted previous frame data is modified by the differential data, and thereby new predicted previous frame data is stored. Furthermore, the predicted previous frame data which is stored in the prediction coding circuit 4 is motion compensated by motion detection data, which has been constructed on the basis of the macro block data S11, to produce predicted current frame data for feeding to the picture data coding circuit 3. Thus, the difference between the macro block data S11 of a frame (current frame) which is to be transmitted and the predicted current frame data S12 is obtained as the differential data S13.

When the motion pictures mentioned referring to FIG. 1 are sent with the construction of FIG. 2, the picture data of the picture PC1 is firstly provided as macro block data S11 at the time t_1 in FIG. 1. In this event, the picture data coding circuit 3 is placed in the intra coding mode, and provides this data as intra coded differential data S13 to the transform coding circuit 5. In this manner, transmission picture data S16 is fed to the transmission buffer memory 8 through the quantizer 6 and the retransform coding circuit 7.

On the other hand, the quantized picture data S15 obtained at the output of the quantizer 6 is prediction coded in the prediction coding circuit 4, and thereby predicted previous frame data which represents the transmission picture data S16 sent to the transmission buffer memory 8 is held in the previous frame memory. When macro block data S11 which represents the picture PC2 at the time t_2 is fed to the picture data coding circuit

3, the predicted previous frame data is motion compensated to produce the predicted current frame data S12, which is provided to the picture data coding circuit 3.

Thus, the picture data coding circuit 3 provides differential data S13 inter coded to the transform coding circuit 5 at the time $t = t_2$. In this manner, the differential data which represents changes in picture between the frames is sent as transmission picture data S16 to the transmission buffer memory 8 while the quantized picture data S15 thereof is provided to the prediction coding circuit 4 to thereby construct and store predicted previous frame data in the prediction coding circuit 4.

Only the differential data representing changes in picture between the frames is sequentially transmitted to the transmission buffer memory 8 by repeating similar operations during the inter coding operation of the picture data coding circuit 3.

The transmission buffer memory 8 accumulates transmission picture data S16 which has been reached in this manner, and successively sends the accumulated transmission picture data S16 as transmission data D_{TRANS} to a transmission line 9 at a data transmission rate which is determined according to the transmission capacity of the transmission line 9.

Concurrently, the transmission buffer memory 8 detects the amount of residual data to feed back residual amount data S17, which changes according to the amount of the residual data, to the quantizer 6, and thereby the quantization step size is controlled according to the residual amount data S17 to regulate the amount of data generated as the transmission picture data S16, so that an appropriate amount of the residual data (not to produce overflow or underflow) is kept in the transmission buffer memory 8.

When the amount of residual data in the transmission buffer memory 8 increases to a permissible upper limit, rough quantization is carried out in the quantizer 6 by enlarging the step size of the quantization step STPS (FIG. 3) of the quantizer 6 on the residual amount data S17, so that the amount of the transmission picture data S16 is reduced.

On the contrary, when the amount of the residual data in the transmission buffer memory 8 decreases to a permissible lower limit, the residual amount data S17 controls the step size of the quantization step STPS of the quantizer 6 to a smaller value, and thus the amount of generation of data of the transmission picture data S16 is increased by executing fine quantization in the quantizer 6.

More specifically, in the transmission system, an evaluation function is detected stepwise by a motion vector detection circuit with reference to a picture of a predetermined frame (hereinafter referred to as reference frame).

Moreover, in the transmission system the picture of the reference frame is shifted by the motion vector to produce a comparison reference picture, and then detects differential data between that comparison reference picture and the picture to be transmitted. The differential data is transmitted together with the motion vector.

In the receiving system, the reference frame picture previously transmitted is moved by the motion vector sent, and then the differential data sent is added to reconstruct the original picture.

In the conventional picture data generating system 1, the transmission buffer memory 8 is, as described, provided as means for transmitting significant picture information while matched to a transmission condition in which the data transmission rate of the transmission data D_{TRANS} is limited according to the transmission capacity of the transmission line 9, and thereby picture data is accumulated in the transmission buffer memory 8 so that the picture data of the transmission capacity of the transmission line 9 may be sent without excess or deficiency. However, it is possible in practice that the transmission buffer memory 8 overflows when the amount of picture data generated in the picture data generating system 1 becomes extremely large.

Moreover, in the picture data generating system 1 of such a construction, there is a problem in that the transmission buffer memory overflows due to an increase of the amount of generation of coded transmission data when moving pictures to be transmitted are rapidly moving picture or contents of thereof changes greatly, for example, as in a change of a scene.

As one technique to solve the problem, there is studied a frame dropping technique in which subsequent frames are not coded when the amount of generation of transmission data is excessively increased.

In a case where rapidly moving pictures are sent for a relatively long time, frame dropping operations are however repeated often since the amount of the generation of the transmission data continues to increase. Thus, there is a problem in that visual smoothness of movement of the reproduced moving pictures is lost, and hence this technique is not still sufficient for sending moving pictures.

Furthermore, incidentally, in such a type of video signal transmission system in inter coding processing, one frame of a picture is divided to a plurality of regions (hereinafter referred to as macro blocks) and a motion vector is detected for each macro block.

More specifically, within a predetermined motion vector detection range the picture of a reference frame is sequentially moved relatively to each macro block, and thereby a shift position (which provides the motion vector) where the differential data is the smallest in amount is detected.

The picture of the reference frame is further moved to the detected shift position to detect picture data of a region which corresponds to the macro block, and thereby picture data of a comparison reference for detection of differential data is produced.

By repeating this processing, the differential data is detected for each macro block, and is then sent after discrete cosine transformation, quantization, variable length coding.

Thus, in such a type of video signal transmission system, there is a case where picture data is coded in such a way that boundaries between macro blocks become obtrusive when a motion vector is detected for each macro block.

To make these boundaries unobtrusive, there has been considered a technique in which in detecting differential data a high frequency zone of picture data for comparison reference is suppressed by means of a filter circuit as disclosed in Japanese Patent Laid-open Publication 60(1985)-206,318, for example.

For making the boundaries unobtrusive by suppressing a high frequency zone of picture data for comparison reference, it is necessary to change the characteristic of the filter according to the position of picture data, and there is hence a problem in that kinds of filter circuits are practically needed for real time processing.

Furthermore, a picture of the reference frame is necessary for an inter coding processing to decode the original picture data.

For this reason, in this type of the video signal transmission system an immediately previous frame, for example, is selected as the reference frame, and picture data intra coded is sent in place of differential data inter coded for each predetermined frame.

The intra coding is a processing to code picture data at a high efficiency using a correlation in the frame and is inferior in transmission efficiency of picture data to the inter coding processing but the original picture can be reconstructed by only the picture data sent.

Accordingly, the original picture data can be reconstructed on the basis of the differential data transmitted if the immediately previous frame is intra coded, and if with that frame selected as the reference frame, picture data of the subsequent frame is inter coded.

Moreover, on the basis of the picture data reconstructed in this manner picture data of the subsequent frame can be also reconstructed.

In such a type of the video signal transmission system, the line is connected after the coding of picture data is commenced.

Thus, inter coding may be repeated just after the line is connected. In this case, any correct picture cannot be reconstructed at the receiving end until picture data intra coded is sent.

More specifically, in a case where picture data intra coded is sent every 128 frames, for example, the speaker at the receiving end must talk, monitoring an unnatural picture displayed for about 13 seconds at maximum when the frame frequency of the picture data is 10 Hz. Thus, there is a problem in facility.

SUMMARY OF THE INVENTION

In view of the foregoing, an object of this invention is to provide a video signal transmission system which prevents an excessively large amount of quantized data from being produced by determining the quantization step size according to the format of picture data to be quantized.

Another object of this invention is to provide a video signal transmission system which performs frame dropping while moving pictures are kept as visually smooth in movement as possible.

Another object of this invention is to provide a filter circuit for using suitably a video signal transmission system.

Another object of this invention is to provide a video signal transmission system which is capable of enhancing facility as compared to the prior art by effectively avoiding unnatural display pictures.

A first aspect of the invention provides a video signal coding method and apparatus in which video signals VD are alternatively intra and inter coded and are then quantized for transforming to picture data, the quantization is, according to the present invention, executed by enlarging the quantization step size QNT to a predetermined rough quantization level QNT = 31 when the picture data to be quantized is in an intra coded format.

When picture data which has been high efficiency coded in an inter or intra coding mode is quantized, the amount of the picture data of which type is inter coded data is extremely large.

When a judged format of picture data to be quantized is an intra coding format, the quantization step size is enlarged. In this manner, it is possible to effectively restrain the amount of picture data generated by the quantization from becoming excessively large.

Moreover, a second aspect of the invention provides a video signal coding system and method which includes a transmission buffer circuit 32. In the video signal coding system, transmission picture data S40 high efficiency coded is temporarily stored in the transmission buffer circuit 32, and the transmission picture data

S40 stored is sequentially outputted to a transmission line 43 according to a data transmission capacity of the transmission line 43, from dropping of the transmission picture data S40 is executed when a data residual amount "Buffer" of the transmission buffer circuit 32 exceeds a predetermined upper limit (QNT = 31); and the frame dropping is completed when the data residual amount "Buffer" of the transmission buffer circuit 32 reduces to a predetermined desired value level MG (QNT = 1) smaller than the upper limit (QNT = 31).

When the data residual amount "Buffer" of the transmission buffer memory 32 exceeds the upper limit (QNT = 31), the frame dropping operation is instructed to be carried out, and then the frame dropping operation is completed when the data residual amount "Buffer" becomes below the desired value MG (QNT = 1) smaller than the upper limit (QNT = 31). In this manner, it is avoided that the frame dropping operation is resumed at once even when the data residual amount "Buffer" is rapidly increased after the previous frame dropping operation is completed, and moreover it is possible to quickly converge the data residual amount "Buffer" at the desired value MG (QNT = 1) when the amount of generation of data decreases after the frame dropping operation is completed.

In this manner, the output pictures can be made smooth in movement and degradation in picture quality thereof can be avoided.

Furthermore a third aspect of the invention provides a vertical digital filter circuit having a plurality of delay circuits 101A and 101B in series, each of the delay circuits 101A and 101B outputting picture data consecutive in the vertical scanning direction; a vertical selection circuit 102A, 102B and 104 for selectively outputting the picture data outputted from the vertical digital filter circuit; a horizontal digital filter circuit having a plurality of delay circuits 107A, 107B and 107C in series, each of the delay circuits 107A, 107B and 107C outputting picture data consecutive in the horizontal scanning direction; and a horizontal selection circuit 108A, 108B and 109 for selectively outputting the picture data outputted from the horizontal digital filter circuit; and wherein: picture data D_{PRI} are sequentially inputted to the vertical digital filter circuit or the horizontal digital filter circuit; the output data D_V or D_H of the vertical selection circuit 102A, 102B and 104 or the horizontal selection circuit 108A, 108B and 109 is fed to the horizontal digital filter circuit or the vertical digital filter circuit; the picture data D_{PRO} outputted from the horizontal selection circuit 108A, 108B and 109 or the vertical selection circuit 102A, 102B and 104 is corrected by switching the selective outputs from the vertical selection circuit 102A, 102B and 104 and the horizontal selection circuit 108A, 108B and 109. The invention also provides a corresponding method of digital filtering.

In the vertical digital filter circuit 101A and 101B, and the vertical selection circuit 102A, 102B and 104, picture data consecutive in the vertical scanning direction are selectively outputted, respectively whereas in the horizontal digital filter circuit 107A, 107B and 107C and the horizontal selection circuit 108A, 108B and 109, picture data consecutive in the horizontal scanning direction are selectively outputted, respectively. In this event, the picture data D_{PRI} is sequentially inputted, and at the same time output data of the vertical selection circuit 102A, 102B and 104 or the horizontal selection circuit 108A, 108B, and 109 is outputted to the horizontal digital filter circuit 107A, 107B and 107C or the vertical digital filter circuit 101A and 101B, and thereby the characteristic of the filter is switched depending on selective outputs from the vertical selection circuit 102A, 102B and 104 and the horizontal selection circuit 108A, 108B, and 109.

Furthermore, a fourth aspect of the present invention provides a video signal transmission system 161 and method in which video signals are transmitted by repeating inter coding and intra coding at a predetermined cycle, according to the present invention the video signals D_{IN} of a predetermined frame are intra coded and then sent after a line L1 is connected to a transmission destination.

When video signals D_{IN} of a predetermined frame are intra coded and then sent after a line L1 is connected to a transmission destination, a picture which was sent just after the line was connected can be reconstructed in the destination, and the speaker may monitor the picture.

A fifth aspect of the invention provides: a video signal transmission system in which video signals are transmitted by repeating inter coding and intra coding at a predetermined cycle, characterized in that: the video signals of predetermined frames are intra coded and then transmitted after a line is connected to a destination; and a corresponding apparatus for performing the method.

A sixth aspect of the invention provides: a video signal coding method in which video signals are alternatively intra and inter coded and are then quantized for transforming to picture data, characterized in that: a power of said picture data is calculated when said picture data to be quantized is a data intra coded, and then said quantization is executed with a quantization step size which is reduced data a predetermined ratio to a quantization step size of a previous frame when said power of picture data calculated is smaller than a predetermined threshold value; and a corresponding apparatus for performing the method.

Any or all of the above aspects of the invention may be combined to provide improved systems and methods.

The invention will be further described by way of non-limitative example with reference to the accompanying

drawings in which like parts are designated by like reference numerals or characters:

FIG. 1 is a schematic diagram for illustrating the inter/intra frame coding;

FIG. 2 is a block diagram illustrating the conventional picture data generating system;

FIG. 3 is a graph showing the quantization step thereof;

5 FIGS. 4A, 4B and 5 are block diagrams illustrating the encoder and decoder which constitutes the picture information transmission system using the video signal coding method according to the present invention;

FIG. 6 is a schematic diagram showing the construction of the frame picture data;

FIG. 7 is a block diagram illustrating the header

data processing system of FIG. 4;

10 data processing system of FIGS. 4A and 4B;

FIG. 8 is a schematic diagram showing the

construction of the flag data of FIG. 7;

construction of the flag data of FIGS. 7A and 7B;

15 FIG. 9A and 9B are flow charts showing the quantization step size determining routine of the quantization control unit 36 of FIG. 4;

FIG. 10 is a graph illustrating changes of residual data in the transmission buffer memory 32 of FIG. 4B;

FIG. 11 is a table showing types of macro blocks;

FIG. 12 is an illustration of the transform coefficient matrix;

20 FIG. 13 is the characteristic curve illustrating changes of the data residual amount of the transmission buffer memory due to the frame dropping according to the second embodiment of the present invention;

FIG. 14 is a graph illustrating the accumulated value of the transmission picture data inputted to the transmission buffer memory;

FIG. 15 is a block diagram illustrating the video signal transmission system according to the third embodiment of the present invention;

25 FIG. 16 is a block diagram showing the differential data producing circuit;

FIG. 17 is a block diagram illustrating the loop filter circuit;

FIGS. 18 to 22 are schematic diagrams showing the operation thereof;

FIGS. 23 and 24 are block diagrams illustrating decoder circuits;

FIGS. 25 and 26 are schematic diagrams illustrating other embodiments;

30 FIG. 27 is a block diagram illustrating the videophone system in accordance to the fourth embodiment of the present invention; and

FIG. 28 is a signal wave form diagram illustrating the operation thereof.

Preferred embodiments of this invention will be described with reference to the accompanying drawings:

35 (1) The whole construction of the picture information transmission system of the first embodiment

In FIGS. 4A, 4B and 5, a picture information transmission system 21 consists of an encoder 21A and a decoder 21B. The encoder 21A preprocesses an input video signal VD_N in an input circuit unit 22 and then sends an input picture data S21, which is a pixel data of 16 by 16 pixels, that is, a pixel data of a macro block
40 MB, from an analog/digital conversion circuit 23 to a pixel data processing system SYM1. At the timing of processing the pixel data in the unit of the macro block MB in each processing step of the pixel data processing system SYM1, a processing information data corresponding to the data to be processed is sequentially transmitted through a header data processing system SYM2. Thus, pixel data and header data are processed by the pipe line technique in the pixel data processing system SYM1 and the header data processing system
45 SYM2, respectively.

In this embodiment, macro block data which is sequentially sent as the input picture data S21 is extracted from frame picture data FRM according to a technique shown in FIG. 6.

50 Firstly, frame picture data FRM of a picture is separated into 2 (horizontal direction) x 6 (vertical direction) of block groups GOB. Each block group GOB contains 11 (horizontal direction) x 3 (vertical direction) of macro blocks MB. Each macro block MB contains 16 by 16 pixels of luminance signal data $Y_{00} - Y_{11}$ (each consisting of 8 by 8 luminance signal data) and chrominance signal data C_b and C_r , which is chrominance signal data corresponding to all the pixel data of the luminance signal data $Y_{00} - Y_{11}$.

Thus, the input picture data S21 which is sent for each macro block MB is fed to a motion compensation circuit 25. The motion compensation circuit 25 compares the input picture data S21 and predicted previous
55 frame data S23 from a predicted previous frame memory 27 in response to a motion detection control signal S22 fed from a motion compensation control unit 26, which is provided in the header data processing system SYM2, and the motion compensation circuit 25 thereby detects motion vector data "MVD(x)" and "MVD(y)", which are supplied as first header data HD1 (FIGS. 7A and 7B) to the motion compensation control unit 26.

Furthermore, the motion compensation circuit 25 constructs predicted current frame data S24 by motion compensating the predicted previous frame data S23 by the motion vector data "MVD(x)" and "MVD(y)" in a motion compensation circuit body 25A. The predicted current frame data S24 is fed to a picture data coding circuit 28 together with the input picture data S21 to be processed.

5 As shown in FIGS. 7A and 7B, the motion compensation control unit 26 identifies each macro block MB, which is sequentially transmitted to each processing step of the pixel data processing system SYM1, by adding the following data as the first header data HD1 for the macro block MB: transmission frame number data "TR Counter" representing a transmission sequence of the frame picture data FRM; block group number data "GOB address" representing the block group GOB (FIG. 6); macro block number data "MB address" representing the
10 macro block MB among the block group GOB. Moreover the motion compensation control unit 26 constructs flag data FLAGS representing a processing or a processing type of the macro block MB to be processed, the motion vector data "MVD(x)" and "MVD(y)" of the macro block MB, and differential data " $\Sigma |A-B|$ " which represents the evaluation.

As shown in FIG. 8, the flag data "FLAGS" can have one word (16 bits) of flags at maximum. A motion compensation control flag "MC on/off" which represents whether or not the macro block MB to be processed
15 should be processed in motion compensation mode is set at bit 0.

At bit 1 of the flag data "FLAGS", inter-frame/intra-frame flag "Inter/Intra" which represents whether the macro block MB to be processed should be in inter coding mode or in intra coding mode is set.

At bit 2 of the flag data "FLAGS", a filter flag "Filter on/off" which represents whether or not a loop filter
20 25B of the motion compensation circuit 25 is used is set.

At bit 3 of the flag data "FLAGS", a transmission flag "Coded/Not-coded" which represents whether or not block data $Y_{00} - C_r$ (FIG. 6) contained in the macro block to be processed should be sent can be set.

At bit 4 of the flag data "FLAGS", a drop frame flag "Drop frame flag" which represents whether or not the macro block MB to be processed is frame dropped can be set.

At bit 5 of the flag data "FLAGS", an forced refreshing flag "Refresh on/off" which represents whether or
25 not the macro block MB to be processed is forcedly refreshed can be set.

At bit 6 of the flag data "FLAGS", a macro block power appreciation flag "MBP appreciate" may be set.

The differential data $\Sigma |A-B|$ represents a minimum value among differences between the macro block data "A" to be processed of current frame data S25 and macro block data "B" compensated by detection motion
30 vectors of the predicted previous frame data S23, and enables appreciation of detected motion vectors.

In the inter coding mode, the picture data coding circuit 28 feeds the current frame data S25, which is provided from the motion compensation circuit 25, as difference data S26 to a transform coding circuit 29 without any change (FIGS. 4A and 4B). On the other hand, in the intra coding mode difference data S26 which is the difference between the pixel data of the current frame data S25 and the pixel data of the predicted current frame
35 data S24 is fed to the transform coding circuit 29.

In the header data processing system SYM2, an inter/intra coding control unit 30 is provided to correspond to the picture data coding circuit 28. According to the first header data HD1, fed from the motion compensation control unit 26, and the operation data S31, supplied from the picture data coding circuit 28, the inter/intra coding control unit 30 operates data necessary for obtaining the inter-frame/intra-frame flag "Inter/Intra" and the filter
40 flag "Filter on/off" (FIG. 8) and sends the resulting data as a second header data HD2 to a filter control unit 31; the inter-frame/intra-frame flag "Inter/Intra" is to indicate the coding mode of the picture data coding circuit 28 whereas the filter flag "Filter" is to control the operation of the loop filter 25B of the motion compensation circuit 25.

As shown in FIGS. 7A and 7B, the second header data HD2 takes over the data which constitutes the first header data HD1; the transmission frame number data "TR Counter" to the differential data " $\Sigma |A-B|$ ". Furthermore, in the inter/intra coding control unit 30, power data which is necessary to construct inter/intra coding mode switching signal S33 and filter on/off signal S34 in the filter control unit 31 is added to the second header data HD2, the power data including " $\Sigma (A)^2(L)$ " and " $\Sigma (A)^2(H)$ ", " $\Sigma (A-B)^2(L)$ " and " $\Sigma (A-B)^2(H)$ ", " $\Sigma (A-FB)^2(L)$ " and " $\Sigma (A-FB)^2(H)$ " and " $\Sigma (A)$ ".

50 The power data " $\Sigma (A)^2(L)$ " and " $\Sigma (A)^2(H)$ " represent the lower bit and the upper bit of the sum of the squares of macro block pixel data "A" of the current frame data S25, respectively. The power data " $\Sigma (A-B)^2(L)$ " and " $\Sigma (A-B)^2(H)$ " represent the lower bit and the upper bit of the sum of the squares of the difference "A-B" of the macro block pixel data "A" of the current frame data S25 and macro block pixel data "B" of the predicted current frame data S24, which is constructed without passing through the loop filter 25B, respectively. The " $\Sigma (A-FB)^2(L)$ " and
55 " $\Sigma (A-FB)^2(H)$ " represent the lower bit and the upper bit of the sum of the squares of the difference "A-FB" of the macro block pixel data "A" of the current frame data S25 and macro block pixel data "FB" of the predicted current frame data S24, which is constructed through the loop filter 25B, respectively. The " $\Sigma (A)$ " represents the sum of the macro block pixel data "A" of the current frame data S25. To evaluate the magnitude of each

data to be processed, the amount of the data is expressed in power value (each sum of the squares is obtained as a value irrespective of sign).

According to the second header data HD2 fed from the inter/intra coding control unit 30 and residual amount data S32 fed from a transmission buffer memory 32, the filter control unit 31 sends an inter/intra coding mode switching signal S33 to the picture data coding circuit 28 and a filter on/off signal S34 to the loop filter 25B, and furthermore the filter control unit 31 adds the filter flag "Filter on/off", representing the contents of the filter on/off signal S34, to the second header data HD2 and hands over the resulting data as third header data HD3 to a threshold control unit 35.

Here, the filter control unit 31 firstly controls the picture data coding circuit 28 to the intra coding mode when transmission data inter frame coded becomes larger in amount than the transmission data intra frame coded.

Secondly, according to the filter on/off signal S34 the filter control unit 31 controls the loop filter 25B not to perform the filtering operation when during the processing in the inter coding mode, the predicted current frame data S24 which has not been processed in the loop filter 25B is smaller in the differential value than the predicted current frame data S24 which has been processed there.

Thirdly, the filter control unit 31 switches the picture data coding circuit 28 to the intra coding mode according to the inter/intra coding mode switching signal S33 in the forced refreshing mode.

Fourthly, the filter control unit 31 detects a state in which the transmission buffer memory 32 is liable to overflow data according to the residual amount data S32 provided from the transmission buffer memory 32 and thereby sends to the threshold control unit 35 the third header data HD3 which contains a flag to command to execute a frame dropping procedure.

Thus, the picture data coding circuit 28 supplies to the transform coding circuit 29 difference data S26 which has been encoded in such a mode that the difference between the current frame data S25 and the predicted current frame data S24 becomes minimum.

As shown in FIGS. 7A and 7B, the third header data HD3 takes over transmission frame number data "TR Counter" to motion vector data "MVD(x)" and "MVD(y)" from the second header data HD2, and the filter control unit 31 adds 6 bits of filter flag "Filter on/off" which correspond to the block data Y_{00} to C_r to the third header data HD3.

The transform coding circuit 29 is a discrete cosine transform circuit and sends to a transmission block setting circuit 34 transformation code data S35 which is obtained by zigzag scanning discrete cosine transformed coefficients per six blocks Y_{00} , Y_{01} , Y_{10} , Y_{11} , C_b and C_r .

The transmission block setting circuit 34 computes the sum of squares of coefficient data in the number of n from the leading data about each of the six block data Y_{00} to C_r (FIG. 6) and hands over the result of the operation as power detection data S36 to the threshold control unit 35.

In this event, the threshold control unit 35 compares the power detection data S36 of each block data Y_{00} to C_r with predetermined threshold and thereby constructs 6 bits of transmission permitted/not-permitted data "CBPN" which represents that the block data is not permitted to be transmitted when the power detection data S36 is smaller than the threshold whereas the block data is permitted to do so when the power detection data S36 is larger than the threshold. This data is added to the third header data HD3 which has been received from the filter control unit 31. The threshold control unit 35 hands over the resulting data to a quantization control unit 36 as fourth header data HD4 and controls the transmission block setting circuit 34 to send corresponding block data Y_{00} to C_r as transmission block patterning data S37 to a quantizer 37.

Here, as shown in FIGS. 7A and 7B the fourth header data HD4 takes over the transmission frame number data "TR Counter" to filter flag "Filter on/off" of the third header data HD3, and 6 bits of the transmission permitted/not-permitted flag "CBPN", which has been generated at the threshold control unit 35 to correspond to the blocks Y_{00} to C_r , is added to the fourth header data HD4.

On the basis of the fourth header data HD4 handed over from the threshold control unit 35 and the residual amount data S32 sent from the transmission buffer memory 32, the quantization control unit 36 performs a quantization step size determination routine RT0 shown in FIGS. 9A and 9B, and thereby provides a quantization step size control signal S38 to the quantizer 37, thus causing the quantizer 37 to perform the quantization procedure at the quantization step size which matches to the data contained in the macro block MB. Consequently, quantized picture data S39 which has been obtained at the output terminal of the quantizer 37 is fed to a variable length coding circuit 38.

In addition to this, according to the fourth header data HD4 the quantization control unit 36, as shown in FIGS. 7A and 7B, constructs as header data HD5 data in which the flag data "FLAGS" and the motion vector data "MVD(x)" and "MVD(y)" are separated and arranged in series to correspond to each of the block data Y_{00} to C_r (FIGS. 6), and the quantization control unit 36 hands the header data HD5 to the variable length coding circuit 38 and an inverse quantizer 40.

As shown in FIGS. 7A and 7B, the header data HD5 takes over the transmission frame number data "TR

Counter" t the macro block MB address in the fourth header data HD4 without any change, and the quantization control unit 36 adds quantization size data "QNT" and flag data "FLAGS" for the block data Y_{00} to C_r and motion vector data $MVD(x)$ and $MVD(y)$ to the header data HD5.

5 The variable length coding circuit 38 performs variable length coding on the header data HD5 and the quantized picture data S39 to construct transmission picture data S40, which is supplied to the transmission buffer memory 32.

In variable length coding the block data Y_{00} to C_r , the variable length coding circuit 38 performs processing to throw away the block data without sending as transmission picture data S40 when "frame dropping" or "transmission not permitted" is instructed according to the corresponding flag data "FLAGS".

10 The transmission buffer memory 32 stores the transmission picture data S40, which is read at a predetermined transmission rate and is composed with transmission voice data S41, sent from a voice data generator 42, in the multiplexer 41 to be sent to the transmission line 43.

The inverse quantizer 40 inverse quantizes the quantized picture data S39, sent from the quantizer 37, according to the header data HD5, and then feeds the inverse quantization data S42 to inverse transform coding circuit 43 for converting to inverse transform coded data S43, which is then fed to a decoder circuit 44. Thus, coded differential data S44 which represents picture information sent as the transmission picture data S40 is supplied to the predicted previous frame memory 27.

In this event, the predicted previous frame memory 27 performs correction of the predicted previous frame data stored using the coded differential data S44 to store as new predicted previous frame data.

20 Thus, in the encoder 21A of the configuration in FIG. 4, the pixel data processing system SYM1 pipelines pixel data in the unit of a macro block MB according to the header information fed from the header data processing system SYM2. Simultaneously with this, header data is transferred in the header data processing system SYM2, and thereby the pixel data is appropriately processed according to needs by performing of addition or deletion of the header data in each process of the header data processing system SYM2.

25 As shown in FIG. 5, in the decoder 21B the transmission data transmitted from the encoder 21A through transmission line 43 is accepted in a transmission buffer memory 52 through a demultiplexer 51 while transmission voice data S51 is received in a voice data receiving unit 53.

The pixel data received in the transmission buffer memory 52 is separated into received picture data S52 and header data HD11 in a variable length inverse transform circuit 54. The received picture data S52 is inverse quantized to form inverse quantized data S53 in an inverse quantizer 55, and is then inverse transformed to inverse transform coded data S54 by discrete inverse transformation in an inverse transform coding circuit 56.

The inverse transform coded data S54 is fed to a decoder circuit 57 together with header data HD12 constructed in the inverse quantizer 55, and is then stored as coded differential data S55 in a frame memory 58.

30 Thus, the pixel data transmitted is decoded in the frame memory 58 on the basis of the coded differential data S55. In a digital/analog conversion circuit 59, the decoded picture data S56 is converted to an analog signal, which is then outputted as an output video signal VD_{OUT} through an output circuit unit 60.

(2) Procedure to determine the Quantization Step Size

40 The quantization control unit 36 executes the quantization step size determining routine RT0, shown in FIGS. 9A and 9B, on each macro block MB, and thereby a quantization step size QNT is selected to adapt to a format of picture data of the macro block MB to be currently processed (referred to as macro block type) to feed as the quantization step size control signal S38 to the quantizer 37. In this manner, the quantizer 37 is controlled not to produce disturbance of the picture according to the type of macro blocks.

45 In this embodiment, the quantizer 37 is, as shown in FIG. 10, designed so that the quantization step size QNT is stepwisely variable from an upper limit $QNT = 31$ to a lower limit $QNT = 1$. The quantization control unit 36 performs an adaptive control in response to the macro block type "Macro Block Type" so that the data residual amount "Buffer" of the transmission buffer memory 32 falls within the variable control range of the quantization step size QNT, that is, the range of the quantization size controllable range QCR.

50 (2-1) Processing in a case where the amount of the residual data is excessive

When entering the quantization step size determining routine RT0 of FIGS. 9A and 9B, in the step SP1 the quantization control unit 36 makes a judgement as to whether or not the data residual amount "Buffer" of the transmission buffer memory 32 is larger than the sum of the margin "Margin" and the quantization size controllable range QCR.

55 When an affirmative result is obtained, this means that the data residual amount "Buffer" of the transmission buffer memory 32 is above the upper limit. In this case, the quantization control unit 36 proceeds to the step SP2, where it supplies the quantization step size control signal S38 to set the quantization step size QNT to the maximum, i.e., $QNT = 31$, to the quantization control unit 36, and then goes to the step SP3, where the quan-

tization step size QNT currently set is stored as a previous frame quantization step size PQNT.

Thus, the quantization control unit 36 completes the quantization step size determining routine RT0 at the step SP4, and thereby the transform code data S35 is quantized at the roughest quantization step size in the quantizer 37.

5 As a result, the amount of data of the quantized picture data S39 generated in the quantizer 37 is controlled to the smallest level, so that the data residual amount "Buffer" of the transmission buffer memory 32 decreases.

This operation is repeated until the affirmative result is obtained at the step SP1, with the result that the residual data in the transmission buffer memory 32 becomes smaller in amount than the sum of the margin "Margin" and the quantization size controllable range QCR, $QCR + \text{Margin}$.

10 (2-2) Processing in the intra coding mode

In such a state, the quantization control unit 36 goes to the step SP5 since a negative result is obtained in the step SP1, and in that step it is judged whether or not the macro block type "Macro Block Type" is an intra coded block and not forced refresh block "not refresh block".

15 Here, the macro block type "Macro Block Type" is, as shown in FIG. 8, represented by the bit 2, the bit 1 and the bit 0 of the flag data "FLAGS" contained in the header data HD4 given from the threshold control unit 35 to the quantization control unit 36. When these bits are "010", the macro block type is an intra coding type. When "000", the macro block type is an inter coding type. When "001", the macro block type is a motion compensated not filtered type "MC-not filtered". When "101", the macro block type is a motion compensated filtered type "MC filtered".

20 When in the step SP5, an affirmative result is obtained, the flag data "FLAGS" is "000" at the bit 2, the bit 1 and the bit 0 thereof and the forced refreshing flag "refresh" at the bit 4 is in the state of logic "0".

Such a state means that the current frame has been greatly changed from the previous frame to such a degree that the macro block type "Macro Block Type" needs to be intra coded. Moreover, the current state is under the condition such that the forced refreshing mode is not specified.

25 If under such conditions, quantization is carried out at a fine quantization step size in the quantizer 37, the amount of data of the quantized picture data S39 generated from the quantizer 37 becomes extremely large, and hence it is liable that the transmission buffer memory 32 overflows eventually.

In this event, the quantization control unit 36 goes to the step SP6, where the quantization step size QNT is set to the upper limit $QNT = 31$. Thus, a processing to restrain the amount of data of the quantized picture data S39 generated from the quantizer 37 is executed, so that overflowing of the transmission buffer memory 32 is previously avoided.

On the contrary, a negative result is obtained in the step SP5, this means that the object to be projected is not an intra coding type or is an intra coding type and generated as the result of forced refreshing. In this case, the quantization control unit 36 does not perform the procedure of the step SP6 but jump this step.

35 (2-3) Processing in the forced refreshing mode

Subsequently, in the step SP7 the quantization control unit 36 makes a judgement as to whether or not the macro block to be processed is a forced refreshing type block.

When an affirmative result is obtained in this step, this tells that it is indicated that forced refreshing should be achieved. In this case, the quantization control unit 36 proceeds to the step SP8, where the previous frame quantization step size PQNT which has been used as quantization step size QNT in the previous quantization is set. Thus, quantization is carried out at the same quantization step size as in the previous frame when it is indicated that the forced refreshing should be executed.

This enables the quality of the picture not to change to such a degree that it provides an eye-sore in effect when the forced refreshing is performed.

45 The forced refreshing is executed in a predetermined cycle irrespective of the contents of the picture, and hence the quantization step size changes as compared to that of the previous frame even though the contents of the picture does not change. This can provide an eye-sore in many cases.

If the quantization step size is not changed when the forced refreshing is indicated, it is possible not to produce any change of the picture which provides an eye-sore in the refreshing.

50 It is to be noted that the same effect as described above can be achieved by selecting a smaller value in place of using the same value as the previous quantization step size.

A reproduced picture is degraded in quality by enlarging the quantization step size when the forced refreshing is indicated without any change in the picture. On the contrary, slight reduction of the quantization step size somewhat improves the reproduced picture in quality, and thereby it is possible that any change of picture does not come to one's notice in effect.

55 When in the step SP7 a negative result is obtained, this means that the forced refreshing is not currently indicated. In this case, the quantizer 37 does not perform any procedure in the step SP8 but jumps the step. (2-4) Processing in a case where the differential data is large in power

Subsequently, in the step SP9 the quantization control unit 36 judges whether or not the macro block type is the inter coding type and the macro block power MBP is larger than a predetermined threshold "Threshold". Here, the macro block power MBP is defined as:

$$MBP = \sum_{i=1}^n (\text{Coeff}(i))^2 \quad \dots (1)$$

When an affirmative result is obtained in the step SP9, this means that it is in a state that there is produced any change such that a reproduced picture does not extremely degraded in quality even if the picture data of the macro block MB is quantized at a somewhat rough quantization step size and then transmitted, since the picture data, that is, the macro block power MBP of the differential data is large.

When a macro block which meets such conditions is discrete cosine transformed in the transform coding circuit 29, the quantization control unit 36 confirms this in the step SP9 and proceeds to the step SP10, where it sets the quantization step size QNT to the most rough value, that is, the upper limit QNT = 31.

When transform code data S35 of a macro block with a macro block power MBP not so large as this is sent, the quantization control unit 36 jumps the step SP10 not to perform the process of the latter.

The macro block power MBP defined by the equation (1) aims to operate weight of each macro block on the basis of the discrete cosine transform coefficient Coeff(i) which is obtained as a result of the discrete cosine transformation in the transform coding circuit 29. The weight of the discrete cosine transform coefficient represents intensity of a transmission signal which has been obtained by the discrete cosine transformation. A large macro block power MBP thus means that the intensity of the transmission signal as signal transmission means is large, and hence even if the transmission signal is sent with some compression, the transmitted information can be reconstructed in a receiving end without being influenced with external noises.

In such a case, the quantization control unit 36 compressed the amount of the quantized picture data S39, which is generated in the quantizer 37, by changing the quantization step size QNT to a larger value, and thereby reducing a load to the transmission line 43.

Incidentally, the discrete cosine transform circuit which constitutes the transform coding circuit 29 performs discrete cosine transformation according to the following equation;

$$F(u, v)$$

$$= \frac{1}{4} C(u) C(v) \sum_{x=0}^7 \sum_{y=0}^7 f(x, y)$$

$$\cos \left[(2x + 1) \cdot u \cdot \frac{\pi}{16} \right]$$

$$\cos \left[(2y + 1) \cdot v \cdot \frac{\pi}{16} \right] \quad \dots (2)$$

The inverse discrete cosine transform circuit which constitutes the inverse transform coding circuit 56 performs inverse discrete cosine transformation according to the following equation:

$$f(x, y)$$

$$= \frac{1}{4} \sum_{u=0}^{7} \sum_{v=0}^{7} f(u, v) C(u) C(v) F(x, y)$$

$$\cos\left[\left(2x + 1\right) \cdot u \cdot \frac{\pi}{16}\right]$$

$$\cos\left[\left(2y + 1\right) \cdot v \cdot \frac{\pi}{16}\right] \dots (3)$$

where x and y represent coordinates of pixels in the macro block (the upper left corner has a coordinate (0, 0); and u and v represent coordinates of coefficients in the discrete cosine transformation.

When u and v equal zero,

$$C(u)C(v) = \frac{1}{\sqrt{2}} \quad (4)$$

and in the other cases,

$$C(u)C(v) = 1 \quad (5)$$

Suppose that X is a picture data matrix in a macro block and C is a transform matrix when discrete cosine transformation is carried out. In the transformation of each of the equation (2) and (3) in the transform coding circuit 29 a picture data matrix X is horizontal transformed to produce a transformed picture data matrix XC^{-1} , and then undergoes vertical transformation to obtain a transformed picture data matrix $C(X)C^{-1}$.

The transformed picture data matrix $C(X)C^{-1}$ thus obtained is, as illustrated in FIG. 12, expressed as an 8 x 8 transformation coefficient matrix including coefficient Coeff(1), Coeff(2), Coeff(3), ... and Coeff(64), and each coefficient Coeff(i) (i = 1 to 64) of the transform coefficient matrix is read from the transform matrix by scanning in the order of i = 1, 2, 3, ... 64 as the lapse of time.

Thus, the picture data of a one macro block is transformed to transform coefficients Coeff(i) (i = 1 to 64) which constitutes the transform matrix, and these transform coefficients are fed as transmission data arranged in series in time to the quantizer 37.

Thus, the transform coefficient data series Coeff(1), Coeff(2), ... and Coeff(64) fed to the quantizer 37 represent not only information to be sent but intensity of signals to be transmitted. As defined by the equation (1), the sum of squares of transform coefficient data (i = 1 to n) contained in the transform coefficient data series Coeff(i) (i = 1, 2, ... 64) is a value obtained by accumulating so that signals to be sent becomes horizontally and vertically equal in intensity. Thus, the equation (1) defines this as the macro block power MBP.

When the transform coefficient matrix as shown in FIG. 12 is obtained in practice by discrete cosine transformation of pixel data, there is a tendency that power is concentrated at the transform coefficient Coeff(1) at the upper left corner, that is, lower degree transform coefficients whereas significant information is not produced in the transform coefficient at the lower right corner, that is, the higher degree transform coefficient. In this manner, compression of transmission data can be achieved by discrete cosine transformation.

If it is confirmed that a macro block power MBP obtained according to the equation (1) is larger than the predetermined threshold "Threshold" when it has been judged in the step SP9 of FIG. 9B that the macro block type "Macro Block Type" is the inter coding type, this means that the differential data in the macro block MB is sufficiently large. It is thus confirmed that rough quantization is sufficient. If the quantization step size QNT is selected to the upper limit in the step SP10 according to such judgement, the differential data is transmitted at a relatively small amount.

(2-5) Processing in the Inter coding mode

When in the step SP11 of FIG. 9B, it is confirmed that the macro block type "Macro Block Type" is the inter coding type, and that the macro block power MBP is smaller than the predetermined threshold "Threshold", the quantization control unit 36 proceeds to the step SP12, where the quantization step size QNT is set to a 1/2 of the previous quantization step size PQNT used in the previous frame. Then, in the step SP13 it is judged whether or not the quantization step size QNT is smaller than the lower limit $QNT = 1$. When the quantization step size QNT is smaller, it is reset to the lower limit in the step SP14. When not smaller, the value is set as the quantization step size QNT without resetting.

Here, as described in connection with the equation (1) the macro block power MBP represents the intensity of the differential data signal of the macro block, and hence when an affirmative result is obtained in the step SP11, the macro block power MBP represents that the difference is small, and that the picture has a small change in contents from the previous frame.

When such picture data is obtained, it shows that the picture to be transmitted is in a state that there is only a change to such a degree that the picture of the previous frame is partially modified without any great change.

Thus, in the step SP12 the quantization control unit 36 reduces the previous quantization step size PQNT of the previous frame to 1/2, which is set as the quantization step size QNT of the current frame. In this manner, the quantization step size is made finer according to the reduced change for the current frame which is small in movement as compared to the previous frame, and the optimum quantization step size can be thus set.

The quantization control unit 36 repeats such reduction of the quantization step size in the steps SP11 and SP12 while pictures with small motions follow, and hence in a case where transmission of pictures with small motions are continued, the quantization step size is converged toward a value to meet this.

Then, in the steps SP13 and SP14 the quantization step size QNT is controlled not to be smaller than 1, and in a case where pictures with small motions are sent the quantization control unit 36 can thereby stably perform quantization in a state in which the quantization step size QNT is converged to the lower limit.

In a case where a negative result is obtained in the step SP11, the quantization control unit 36 judges that the picture to be sent currently is large in change, and does not perform and jumps the procedures in the steps SP12, SP13 and SP14.

(2-6) The operation of the quantization control unit 36

In the first case where the data residual amount "Buffer" of the transmission buffer memory 32 exceeds the upper limit (QCF + Margin), the quantization control unit 36 detects this in the step SP1 and sets the quantization step size QNT of the quantizer 37 to the upper limit QNT = 31 in the step SP2, so that the data residual amount "Buffer" of the transmission buffer memory 32 is reduced to thereby keep in a state below the upper limit thereof.

In the second case where in this state, block data of which macro block type "Macro Block Type" is the intra coding type and which is not a forced refreshing type is provided to the quantizer 37, the quantization control unit 36 confirms this in the step SP5 and sets the quantization step size QNT of the quantizer 37 to the upper limit QNT = 31 in the step SP6 so that the transmission buffer memory 32 does not overflow.

When negative results are obtained in respective steps SP7, SP9 and SP11 in such an operation mode, the quantization control unit 36 sets the quantization step size which has been set in the step SP6 as previous frame quantization step size PQNT in the step SP3 and then completes the routine.

In the third case where macro block data having the forced refreshing block type is provided to the quantizer 37, in the quantization step size determining routine RT0 the quantization control unit 36 confirms this by the loop of the steps SP1-SP5-SP7. The quantization control unit 36 sets the previous frame quantization step size PQNT as the quantization step size QNT of the quantizer 37 in the step SP8 and thereby controls the picture to be sent not to change in quality from the picture of the previous frame in the forced refreshing mode so that any change in quality which provides an eye-sore is not produced in the forced refreshing.

In this case, the quantization control unit 36 obtains negative results in respective steps SP9 and SP11, and thus the quantization step size QNT which has been set in the step SP8 is set as the previous frame quantization step size PQNT in the step SP3 and then completes the routine.

In the fourth case where picture data of a macro block with a large macro block power MBP is provided to the quantizer 37, in the quantization step size determining routine RT0 the quantization control unit 36 confirms this by the loop of the steps SP1-SP5-SP7-SP9. Then, the quantization control unit 36 sets the quantization step size QNT of the quantizer 37 to the upper limit QNT = 31, and thereby holds the amount of data generated in the quantizer 37 at a small value. This enables the picture data to be transmitted with much improved efficiency.

After such procedures, the quantization control unit 36 obtains a negative result in the step SP11 and thus resets the quantization step size QNT, which has been set in the step SP10, as the previous frame quantization step size PQNT in the step SP3. Then, the routine is completed.

In the fifth case where macro block data which is of the inter coding type with a small macro block power MBP is fed to the quantizer 37, in the quantization step size determining routine RT0 the quantization control unit 36 confirms this by the loop of the steps SP1-SP5-SP7-SP9-SP11. Then, in the step SP12 the value of 1/2 of the previous frame quantization step size PQNT is set as the quantization step size QNT and thereby the quantization step size is converged toward the lower limit QNT = 1.

Thus, the quantization step size which is most suitably applied to the macro block power MBP can be set.

(3) Modifications of the first embodiment

(3-1) Although it is stated that the quantization step size QNT is set to the upper limit $QNT = 31$ in the steps SP6 and SP10 in FIGS. 9A and 9B, the quantization step size QNT is not limited to that upper limit and may be set to other values. It is essential that a rough quantization value which enables rough quantization is selected.

(3-2) It is described that the same threshold "Threshold" is selected for judging the magnitude of the macro block power MBP in the steps SP9 and SP11 of FIG. 9B. By selecting a different value in place of this, an effect similar to the case above described can be achieved.

(3-3) It is further described that in determining the quantization step size QNT from the previous frame quantization step size PQNT in the step SP12 in FIG. 9B, a value of $1/2$ thereof is set. The ratio is not restricted to $1/2$ but may be changed to different values according to needs. It is essential that the quantization step size is set to a size which is obtained by reducing the previous frame quantization step size at a predetermined ratio.

(3-4) It is stated that the quantization step size QNT is converged toward the lower limit $QNT = 1$ in the steps SP13 and SP14 of FIG. 9B. However, the convergence value is not limited to that lower limit but may be set to different values according to needs.

(4) Frame Dropping in the Embodiment

In the picture information transmission system 21 shown in FIGS. 4A and 4B, the transmission buffer memory 32 feeds back the residual amount data S32 representing data residual amount "Buffer" to the quantization control unit 36, and thereby the transmission buffer memory 32 is controlled not to overflow or underflow data by changing the quantization size data QNT in the quantization of the quantizer 37.

More specifically, in the second embodiment the quantizer 37 is as shown in FIG. 13 variable in steps, as a table of the quantization size data QNT, from an upper limit $QNT = 31$ to a lower limit $QNT = 1$. In a case where the data residual amount "Buffer" of the transmission buffer memory 32 approaches the sum of the margin "Margin" and the quantization size controllable range QCR (the permissible upper limit of the data residual amount), the QNT is roughened (that is, changed toward $QNT = 31$).

Accordingly, the amount of data of the quantized picture data S39 is controlled to a small value by carrying out quantization of the transformation code data S35 with the rough quantization step size, and thereby the data residual amount "Buffer" of the transmission buffer memory 32 decreases.

On the contrary, when the data residual amount of the transmission buffer memory 32 becomes small, the quantization control unit 36 changes the QNT to a fine value (that is, toward $QNT = 1$) according to this decrease, and thereby controls the data residual amount "Buffer" of the transmission buffer memory 32 to converge to a level of a desired value MG ($QNT = 1$) always.

The residual amount data S32 fed back from the transmission buffer memory 32 is inputted to the filter control unit 31, and thereby the filter control unit 31 judges whether or not frame dropping is executed in the unit of a field, always monitoring the data residual amount "Buffer" of the transmission buffer memory 32.

More specifically, the filter control unit 31 judges that the transmission buffer memory 32 comes close to an overflow state at a time t , (FIG. 13) when the amount of generation of the transformation code data S35 increases and exceeds the upper limit (margin "Margin" + quantization size controllable range QCR) over which the data residual amount "Buffer" of the transmission buffer memory 32 is not controllable by the quantizer 37. The filter control unit 31 thus sets the drop frame flag "Drop frame flag" (FIG. 8) to "1"; the drop frame flag is contained in flag data "FLAGS" of second header data HD2 of each macro block MB corresponding to one field of pixel data of the subsequent third frame FRM2. This drop frame flag is successively transferred to the third header data HD3, HD4 and HD5, and is thereby sent to the variable length coding circuit 38 and the inverse quantizer 40.

In a case where the drop frame flag "Drop frame flag" which is contained in the flag data "FLAGS" of the header data HD5 inputted to the variable length coding circuit 38 is set to "1", the variable length coding circuit 38 does not send the transmission picture data S40 by not variable length coding the quantized picture data S39.

In this manner, the threshold control unit 35 sets the drop frame flag "Drop frame flag" to "1" about every macro block MB of the second frame FRM2, and thereby the frame FRM2 is frame dropped by controlling the variable length coding circuit 38 not to send the transmission picture data S40 of every macro block MB of the frame FRM2.

Thus, in the transmission buffer memory 32 at a state in which the data residual amount "Buffer" exceeds the upper limit, the data residual amount "Buffer" decreases by data outputted to the transmission line 43 since the one frame of data is not inputted.

On the other hand, the inverse quantizer 40 does not inverse quantize quantized picture data S39 inputted to correspond to header data HD5 when the drop frame flag "Drop frame flag" of the header data HD5 inputted is set to "1", and thereby the voice data generator 42 is not transmitted.

Accordingly, every macro block MB of one frame of the frame FRM2 to which is indicated frame dropping is not outputted as the inverse quantization data S42, so that the data of the frame FRM2 is frame dropped from predicted previous frame data which is to be newly stored in the predicted previous frame memory 27.

Thus, also in the predicted previous frame data the pixel data undergoes frame dropping through the transmission buffer memory 32 to correspond to the frame dropping of the pixel data outputted.

After starting the indication of frame dropping according to the data residual amount "Buffer" of the transmission buffer memory 32, the filter control unit 31 continues to indicate the frame dropping until the data residual amount "Buffer" decreases below the desired residual value MG.

Accordingly, the frame dropping is continued even when the data residual amount "Buffer" of the transmission buffer memory 32 drops below the upper limit at time t_2 (FIG. 13). When the data residual amount "Buffer" is below the desired value MG in a fourth frame FRM4 at time t_3 , the transmission buffer memory 32 detects this, and sets the drop frame flag "Drop frame flag" of header data, corresponding to the subsequent frame FRM5, to "0" after the indication of the frame dropping of every macro block MB of the frame FRM4 on which frame dropping is executed is completed. Thus, variable length coding of quantized picture data S39 is restarted in the frame picture data FRM.

Accordingly, the data residual amount "Buffer" of the transmission buffer memory 32 changes depending on the amount of inputted and outputted data by inputting data from the transmission picture data S40 of this frame FRM5 to the transmission buffer memory 32 again.

Thus, the transmission buffer memory 32 resets the drop frame flag "Drop frame flag" which corresponds to every macro block MB in the unit of a frame to "0" unless the data residual amount "Buffer" exceeds the upper limit again, so that transmission picture data S40 is inputted to the transmission buffer memory 32 and the data residual amount "Buffer" changes accordingly.

Even if the amount of generation of the transmission picture data S40 rapidly increases as in the previous state before the frame dropping was executed, frame dropping is not restarted at once since in the transmission buffer memory 32 the data residual amount "Buffer" has been reduced to the desired value MG.

Thus, a state in which transmitted frames and not-transmitted frames are repeated every other frame is avoided, and hence video images which are obtained by reproducing pixel data outputted from the transmission buffer memory 32 are not deteriorated in smoothness of visual movement.

Because the data residual amount "Buffer" is reduced to the desired value MG (QNT = 1) by frame dropping, the data residual amount "Buffer" can be converged at the desired value MG (QNT = 1) in much shorter time in a case where the amount of generation of the transmission picture data S40 is reduced in the subsequent frame FRM6, for example. In this case, the data residual amount "Buffer" has not yet increased to the upper limit.

When a swift picture (that is, a picture with a large transmission picture data amount) is rapidly changed to a slow picture (that is, a picture with a small transmission picture data amount), the quantization step is controlled to a fine one (QNT = 1) in a short time, and thereby fine picture expression can be given at once when the movement of the picture becomes slow.

It is to be noted that a swift picture cannot be recognized as visual picture being degraded, and that a slow picture can be visually sharply recognized to fine portions thereof. The deterioration of picture quality can be visually avoided by changing the quantization step size to a fine one at once when movement of the picture becomes slower.

FIG. 14 illustrates an accumulated value TRM of the amount of transmission picture data (that is, variable length coded data), inputted to the transmission buffer memory 32, of each frame; FD11 to FD26 designate the amount of transmission picture data of one frame for frames FRM11 to FRM26, respectively.

When in the frame FRM 16, for example, a transmission picture data amount FD16 of one frame is inputted and the data residual amount "Buffer" exceeds the upper limit (QNT = 31), frame dropping is started simultaneously with the completion of inputting of all the data of the frame FRM16, and thereby the data residual amount "Buffer" relatively reduces.

As a result, the data residual amount "Buffer" of the transmission buffer memory 32 reduces below the desired value MG (QNT = 1) before transmission picture data FD17 of a frame FRM17 is inputted, and hence inputting of the transmission picture data of the frame FRM17 is started.

In this event, there may be a case where the transmission picture data amount FD17, FD18, FD19 of each of the subsequent frames FRM17, FRM18 and FRM19 is small and the data residual amount "Buffer" of the transmission buffer memory 32 is below an underflow level UNDER before transmission picture data of a frame FRM20 is inputted. In such a case, stuffing bits are inserted between the data before the "Buffer" becomes

below the underflow level UNDER s that the transmission buffer memory 32 may not underflow.

Thus, in the transmission buffer memory 32 frame dropping and stuffing bit inserting technique are used so that the data residual amount "Buffer" may be overflow or underflow, and thereby the data residual amount "Buffer" is controlled to converge to the desired value (QNT = 1) as closely as possible.

5 According to the construction above, frame dropping is carried out to converge the data residual amount "Buffer" of the transmission buffer memory 32 to desired value MG (QNT = 1), and thus in reproduction of the output data of the transmission buffer memory 32, video images with visually much smooth movement can be obtained and degradation in picture quality can be avoided.

10 (5) Modifications of the second embodiment

(5-1) Although in the second embodiment above described, it is stated that the desired value MG (QNT = 1) is used as the detection level of the end of the frame dropping, but the present invention is not limited to this. For example, the macro block MB may be modified to other levels within the quantization size controllable range
15 QCR, depending on the tendency of the amount of generation of transmission picture data according to swift video images or slow video images.

(5-2) Furthermore, in the above embodiment it is described that the indication of frame dropping is carried out in the filter control unit 31 by detecting the data residual amount "Buffer" of the transmission buffer memory 32, but the present invention is not limited to this. The detection and the indication may be performed in other
20 data processing units provided in previous stages of the transmission buffer memory 32.

(5-3) In the above embodiment, there is described a case where the frame dropping is executed in the variable length coding circuit 38, but the present invention is not restricted to this. It is essential that the frame dropping is performed in steps previous to the transmission buffer memory 32. For example, in the quantizer 37, frame dropping may be carried out by detecting the frame dropping indication of the header data.

25 (5-4) In the embodiment above described, it is stated that the present invention is applied to the picture information transmission system which transmits voice signals and video signals. The present invention is not limited to this and may be widely applied to cases such as a case in which video signals undergo high efficiency coding and are then transmitted.

30 (6) The third embodiment

(6-1) Construction of the third embodiment

In FIG. 15, 65 generally designates a videophone system of the third embodiment of present invention, which transmits pictures and voices of communicators to and from a destination.

35 The video signal transmission system 65 takes a picture of a speaker through a television camera 66, and the video signals S_V outputted from the television camera 66 are provided to a video signal processing circuit 67.

The video signal processing circuit 67 converts the video signals S_V to luminance signals and chrominance signals, which are then converted to digital signals in an analog to digital conversion circuit.

40 Moreover, the video signal processing circuit 67 converts the luminance signals and the chrominance signals which have been converted to digital signals to signals in a format according to CCITT (International Telegraph and Telephone Consultative Committee).

More specifically, after the frame frequency is converted to 15 Hz by thinning video signals for every predetermined frames, the number of pixels in vertical and horizontal scanning directions is reduced.

45 In this manner, with respect to the luminance signals input video signals are constructed having consecutive picture data D_{IN} with 352(horizontal) x 288(vertical) pixels (that is, CIF picture size) or 176 x 144 pixels (QCIF picture size).

Thus, the amount of data is reduced by applying the preliminary processing to the video signals S_V through the video signal processing circuit 67, and thereby the input video signals having consecutive picture data D_{IN}
50 in the order of the line scanning are obtained.

As shown in FIG. 15, a motion vector detection circuit 68 temporarily stores the picture data D_{IN} in a memory circuit in a scan conversion circuit incorporated therein, and then reorders the array of the picture data D_{IN} by sequentially reading in a predetermined order.

55 More specifically, the motion vector detection circuit 68 separates one frame of a picture into 2 x 6 block groups GOB in horizontal and vertical scanning directions, respectively (FIG. 6).

Furthermore, the motion vector detection circuit 68 separates each block group GOB into 11 x 3 macro blocks MB, and then separates each macro block MB into data blocks DB in the unit of 8 x 8 pixels in the horizontal and vertical scanning directions, respectively (FIG. 6).

Thus, in the video signal processing unit, picture data is transferred and processes in the unit of a block group GOB.

In the array of the picture data D_{IN} within each block group GOB, picture data D_{IN} are consecutively arranged in the unit of a macro block MB; within each macro block MB picture data D_{IN} are consecutively arranged in the unit of a data block DB in the order of the raster scanning.

In each macro block MB, 8 x 8 pixels of picture block data (Y_{00} , Y_{01} , Y_{10} and Y_{11}) which are consecutive in the horizontal and vertical scanning directions are provided as a unit to the luminance signal whereas in the video signal processing circuit 67 the two chrominance signals are reduced in the amount of data and are then time-multiplexed and 16 x 16 pixels of data is allotted to respective data blocks DB(C_r , C_b).

In this event, the motion vector detection circuit 68 detects a motion vector for each macro block MB by setting a picture of the immediately previous frame which has been reconstructed in a decoder circuit 69 as the reference frame.

Furthermore, the motion vector detection circuit 68 moves the picture of the reference frame by the detected motion vectors and constructs picture data of 16 x 16 pixels at positions corresponding to macro blocks MB of the current frame. Then, the motion vector detection circuit 68 outputs the picture data D_{PRI} to a differential data construction circuit 70.

Simultaneously, the motion vector detection circuit 68 outputs the picture data D_{IND} , of which array has been rearranged, with a delay necessary for detecting motion vectors.

Moreover, the motion vector detection circuit 68 generates a header D_{HET} on the basis of the number of the frame of the picture data D_{IND} , address data of the block group and the macro block, motion vector D_{UG} , and a sum of an absolute value obtained in detection of the motion vector and outputs the header to the differential data construction circuit 70.

The differential data construction circuit 70 outputs picture data D_{IND} for every predetermined frames to a subsequent discrete cosine transform circuit 71 without processing it, so that intra coded picture data is transmitted to a transmission destination at predetermined time intervals.

Regarding frames other than frames intra coded, picture data D_{PRI} is subtracted from the picture data D_{IND} , and the resultant differential data D_z is outputted to the discrete cosine transform circuit 71.

In the video signal transmission system 65, picture data is thus inter coded by sending the differential data D_z , and intra and inter coding operations are switched at a predetermined cycle. In this manner, the input video signals are efficiently transmitted to a destination.

In this event, the differential data construction circuit 70 suppresses a high frequency component of the picture data D_{PRI} with a loop filter circuit according to needs when the picture data D_{PRI} is subtracted from the picture data D_{IND} .

This makes the boundaries between macro blocks MB unobtrusive when differential data D_z is coded by detecting the motion vector in the unit of a macro block MB.

Moreover, the differential data construction circuit 70 detects the amount of data necessary for transmission in the unit of a macro block MB. When the differential data construction circuit 70 judges that the macro block MB can be transmitted at a small amount of data by intra coding as compared to inter coding, even a macro block MB of a frame to be inter coded is outputted to the following discrete cosine transform circuit 71 without performing any operation on the picture data D_{IND} as in the macro block MB of a frame intra coded and then sent.

In the video signal transmission system 65, a high frequency component of motion vector D_{UG} is suppressed according to the amount of data necessary for transmission when the inter coding is performed, and the intra coding operation may be switched from the inter frame operation. In this manner, the video signals are efficiently sent using the technique of the selective prediction.

Simultaneously, the differential data construction circuit 70 remove data of the absolute sum from the header D_{HET} sent from the motion vector detection circuit 68, and then adds discrimination data of the inter coding and intra coding and discrimination data as to whether or not the differential data is obtained through the loop filter circuit for outputting to the discrete cosine transform circuit 71.

The discrete cosine transform circuit 71 discrete cosine transforms the picture data D_{IND} and the differential data D_z , which have been outputted from the differential data construction circuit 70, in the unit of a macro block MB, using a two dimensional autocorrelation between video signals. The resulting transformed data D_{DCT} is outputted to a quantizer 72.

In this event, the discrete cosine transform circuit 71 adds data, such as accumulated code length of the transformed data D_{DCT} , to the header sent from the differential data construction circuit 70 and then output it.

The quantizer 72 quantizes and then outputs the transformed data D_{DCT} .

In this event, the quantizer 72 detects the accumulated code length and the amount of data of the transformed data D_{DCT} according to the header outputted from the discrete cosine transform circuit 71, and at the

same time detects a residual amount of the transmission buffer circuit 73. According to the result of the detection, the quantization step size is changed.

In this manner, the quantizer 72 keeps the amount of data at a predetermined value per each frame to be transmitted.

5 Furthermore, the quantizer 72 deletes data, such as the accumulated code length of the transformed data D_{DCT} , from the header outputted from the discrete cosine transform circuit 71, and then adds data of the quantization step size to the header for outputting.

The inverse quantization circuit 74 performs transformation inverse to the quantizer 72 according to the header outputted from the quantizer 72, and thereby reconstructs the transformed data D_{DCT} of the differential data construction circuit 70, which is to be reproduced in the transmission destination, at the transmission end.

10 On the other hand, the inverse discrete cosine transform circuit 75 executes a transformation operation inverse to the discrete cosine transform circuit 71 according to the header sent through the inverse quantization circuit 74.

Thus, in the video signal transmission system 65, the input data of the discrete cosine transform circuit 71 which is reconstructed in the destination is reproduced in the transmission end.

More specifically, through the inverse discrete cosine transform circuit 75, the picture data D_{IND} can be reconstructed on video signals intra coded and transmitted whereas the differential data D_z can be reproduced on video signals inter coded and sent.

A decoder circuit 69 is composed of a frame memory circuit and an adder circuit, and the operation thereof is switched according to the header transmitted through the inverse discrete cosine transform circuit 75.

More specifically, when intra coded data (that is, picture data which reconstructs the picture data D_{IND}) is outputted from the inverse discrete cosine transform circuit 75, the decoder circuit 69 directly stores the picture data to the frame memory circuit.

25 The picture data D_{SV} stored in the frame memory circuit is outputted to the motion vector detection circuit 68 at the timing of inputting picture data D_{IN} of the next frame to the motion vector detection circuit 68.

In this manner, in the motion vector detection circuit 68 a motion vector of the frame subsequent to the intra coded frame can be detected on that intra coded frame as the reference frame.

When inter coded data (that is, data which reconstructs the differential data D_z) is outputted from the inverse discrete cosine transform circuit 75, the decoder circuit 69 shifts the picture data D_{SV} stored in the frame memory circuit by the motion vector of the differential data D_z , and then adds the shifted picture data to the differential data D_z . The resultant data is stored in the frame memory circuit.

Thus, the original picture data of the frame inter coded can be reconstructed. In this manner, pictures sent to the destination are sequentially reconstructed and stored in the frame memory circuit.

35 Furthermore, The decoder circuit 69 outputs the picture data D_{SV} stored in the frame memory circuit to the motion vector detection circuit 68 at the timing of inputting picture data D_{IN} of the next frame to the motion vector detection circuit 68.

This enables motion vectors of current frames to be sequentially detected on the basis of respective immediately previous frames in the motion vector detection circuit 68.

40 In this event, in the decoder circuit 69, a high frequency component of the differential data D_z which has been produced through the loop filter circuit is suppressed by means of the loop filter circuit and the differential data D_z is shifted by the motion vector. Thus, the loop filter circuit is changed in relation to the differential data construction circuit 70 so that the boundaries between macro blocks MB are not unobtrusive.

A variable length coding circuit 76 applies variable length processing to the output data of the quantizer 72 together with data, such as the motion vector, the output data being obtained through the buffer circuit 77. 45 Then, the variable length coding circuit 76 outputs the resultant data to the transmission buffer circuit 73 together with the header.

The transmission buffer circuit 73 temporarily stores and then sequentially outputs the output data of the variable length coding circuit 76.

50 A stuff bit adding circuit 78 outputs the output data of the transmission buffer circuit 73 to a error correction circuit 79. In this event, the stuff bit adding circuit 78 detects the amount of input/output data of the transmission buffer circuit 73. When the amount of input data of the transmission buffer circuit 73 becomes extremely small as compared to a transmission rate of the line L1, the stuff bit adding circuit 78 inserts stuff bits in data at predetermined timings.

55 The error correction circuit 79 generates a BCH code (bose chaudhuri hquenghem code) according to the output data of the stuff bit adding circuit 78. The error correction circuit 79 adds the code to the output data from the stuff bit adding circuit 78 and outputs the resulting data.

Furthermore, the error correction circuit 79 performs error correction on data obtained from the destination through a multiplex conversion circuit 80 according to the BCH code transmitted by adding the data, and

thereby degradation in picture quality is effectively avoided if an error or errors occur during transmission.

The multiplex conversion circuit 80 multiplexes digital voice signals to the output data of the error correction circuit 79 and then outputs the resulting signals to the line L1.

This enables video signals S_V and voice signals to be efficiently sent to the transmission destination.

5 Simultaneously, the multiplex conversion circuit 80 inputs data transmitted from the destination through the line L1, and separates multiplexed video and digital voice signals.

Furthermore, the multiplex conversion circuit 80 outputs separated digital voice signals to a predetermined decoding circuit, and outputs the video signals to a stuff bit removing circuit 81.

10 The stuff bit removing circuit 81 removes the stuff bits which have been inserted in the stuff bit adding circuit 78 at the destination.

A buffer circuit 82 temporarily stores the stuff bits removed data, and then outputs it to a decoding circuit 83 after the header is separated.

The decoding circuit 83 performs a processing inverse to the processing of the variable length coding circuit 76 at the destination.

15 An inverse quantization circuit 84 performs inverse quantization on the output data of the decoding circuit 83 according to the header inputted through the decoding circuit 83, and thereby reconstructs the input data inverse quantized of the quantizer 72 at the destination.

Similarly with the inverse discrete cosine transform circuit 75, an inverse discrete cosine transform circuit 85 processes the output data of the inverse quantization circuit 84 according to the header, and thereby reconstructs data discrete cosine transformed at the destination.

20 A decoder circuit 86 performs an operation similar to the operation of the decoder circuit 69 according to the header transmitted, and thus picture data encoded at the destination is reconstructed.

A video signal processing circuit 87 executes an operation inverse to the operation of the video signal processing circuit 67 by a technique of interpolate operation, and then outputs the resulting video signals to a monitor 88, so that a picture to be communicated which has been sent from the destination can be monitored.

(6-2) Differential data producing circuit

As shown in FIG. 16, the differential data construction circuit 70 inputs picture data D_{IND} outputted from the motion vector detection circuit 68, to a switch circuit 91 through a buffer memory circuit 92.

25 Thus, the differential data construction circuit 70 outputs picture data D_{IND} to the subsequent discrete cosine transform circuit 71 through the switch circuit 91 and the buffer memory circuit 93 when video signals intra coded are sent.

An arithmetic and logic circuit 94 of a subtraction circuit configuration subtracts picture data D_{PRI} from picture data D_{IND} to produce differential data D_z , which is outputted to a switch circuit 95 through a buffer memory circuit 96.

35 Thus, the differential data construction circuit 70 outputs differential data D_z to the subsequent discrete cosine transform circuit 71 by switching contacts of the switch circuits 91 and 95 when inter coded video signals are transmitted.

An arithmetic and logic circuit 97 of a subtraction circuit configuration accepts picture data D_{PRI} through a loop filter circuit 98 to subtract the picture data D_{PRI} from the picture data D_{IND} to produce differential data D_{FZ} .

40 Furthermore, the arithmetic and logic circuit 97 outputs the differential data D_{FZ} to the switch circuit 95 through the buffer memory circuit 99, and the contact of the switch circuit 95 is switched so that the differential data D_{FZ} may be outputted to the discrete cosine transform circuit 71 in place of the differential data D_z .

As shown in FIG. 17, the loop filter circuit 98 has delay circuits 101A and 101B connected in series and provides picture data D_{PRI} to the delay circuit 101A.

45 As illustrated in FIG. 18, the delay circuits 101A and 101B are each built by connecting eight stages of flip-flop circuit which operate according to the clock frequency of the picture data D_{PRI} . Thus, picture data D_{PRI} which is sequentially inputted at the timing of raster scanning is delayed in the unit of each data block for the time interval of one horizontal scanning of the data block.

Accordingly, in input data D_{PRI} of the delay circuit 101A and output data of delay circuit 101B, picture data 50 D_{PRI} (hereinafter referred to as picture data of the next line and the previous line, respectively) of pixels which are adjacent to output data of the delay circuit 101A (hereinafter referred to as picture data of a current line) in the vertical scanning direction and in a direction reverse to the vertical scanning direction is sequentially arranged.

In a selection circuit 102A, picture data D_{PRI} of the current line and the next line are inputted to contacts 55 P1 and P2 whereas in a selection circuit 102B picture data D_{PRI} of the current line and the previous line to contacts P1 and P2.

Furthermore, the selection circuits 102A and 102B switch their contacts according to switch signals SEL1 and SEL2 outputted from a control circuit 103, and selection outputs thereof are added in an adder 104.

More specifically, as shown in FIGS. 19 and 20, the selection circuits 102A and 102B select contacts P1 during the time interval in which the picture data D_{PRI} of the first line AR1, AR2 and AR3 and the last line AR7, AR8 and AR9 of a data block DB is outputted from the delay circuit 101A.

Thus, doubly weighted picture data D_{PRI} (designated by $A_{0,0}$) of the current line can be obtained through the adder 104 during the time interval.

On the other hand, the selection circuits 102A and 102B select contacts P2 while picture data D_{PRI} of the remaining regions AR4, AR5 and AR6 are outputted from the delay circuit 101A.

In this manner, addition data ($A_{0,-1} + A_{0,1}$) of picture data D_{PRI} (designated by $A_{0,-1}$, $A_{0,1}$, respectively) of the next line and the previous line can be obtained through the adder 104 during this time interval.

A multiplier 105 doubles picture data D_{PRI} of the current line, and then adds the resulting data to output data D_o of the adder 104 at an adder 106.

Thus, in output data D_{vo} of the adder 106, quadruply weighted picture data $4A_{0,0}$ is obtained during the time interval in which the picture data D_{PRI} of the regions AR1, AR2, AR3, AR7, AR8 and AR9 is outputted from the delay circuit 101A.

On the other hand, addition data ($A_{0,-1} + 2A_{0,0} + A_{0,1}$) obtained by adding the doubly weighted picture data $A_{0,0}$ of the current line to the addition data ($A_{0,-1} + A_{0,1}$) is obtained during the time interval in which the picture data D_{PRI} of the remaining regions AR4, AR5 and AR6 are outputted from the delay circuit 101A.

Delay circuits 107A, 107B and 107C consist of flip-flop circuit actuated by the clock frequency of the picture data D_{PRI} , respectively, and are connected in series, in which state output data D_{vo} of the adder 106 is inputted to one end thereof.

Accordingly, picture data D_{PRI} of pixels (hereinafter referred to as picture data of the next pixel and the previous pixel and designated by $A_{1,-1}$, $A_{0,-1}$, $A_{1,-1}$ and $A_{1,1}$, $A_{0,1}$, $A_{1,1}$, respectively) which are adjacent to output data D_{PRI} of the delay circuit 107B (hereinafter referred to as picture data of current pixel and the picture data of the current pixel is designated as $A_{1,0}$, $A_{0,0}$, and $A_{1,0}$ among picture data of the previous line, the current line and the next line) in the horizontal scanning direction and in a direction reverse to the horizontal scanning direction is obtained through the delay circuit 107A and the delay circuit 107C.

In a selection circuit 108A the picture data D_{PRI} of the current pixel and the next pixel are inputted to contacts P1 and P2 while a selection circuit 108B inputs the picture data D_{PRI} of the current pixel and the previous pixel.

Furthermore, the selection circuits 108A and 108B switch their contacts according to switch signals SEL3 and SEL4 outputted from the control circuit 103, and add their selection outputs at an adder 109.

More specifically, the selection circuits 108A and 108B select contacts a during the time interval in which picture data D_{PRI} of the data block DB at the horizontal scanning start positions AR1, AR4 and AR7 and the horizontal scanning end positions AR3, AR6 and AR9 are outputted from the delay circuit 107B.

Thus, eight-fold weighted picture data $8A_{0,0}$ of the current pixel is obtained during the time interval of outputting picture data D_{PRI} of the regions AR1, AR3, AR7 and AR8.

On the other hand, adding data ($2A_{0,-1} + 4A_{0,0} + 2A_{0,1}$) doubly weighting the output data D_{vo} of the adder 106 is obtained during the time interval of outputting picture data D_{PRI} of the region AR4 and AR6 as picture data of the current pixel.

During the time interval in which picture data D_{PRI} of the remaining regions AR2, AR5 and AR8 is outputted as picture data D_{PRI} of the current pixel, the selection circuits 108A and selection circuit 108B select contacts P2.

Thus, quadruply weighted addition data ($4A_{1,0} + 4A_{1,0}$) of picture data $A_{1,0}$ and $A_{1,0}$ of the next and previous pixel is obtained through the adder 109 during the time interval of outputting picture data D_{PRI} of the region AR2 and AR8 as picture data of the current pixel.

On the other hand, addition data ($A_{1,-1} + 2A_{1,0} + A_{1,1} + A_{1,-1} + 2A_{1,0} + A_{1,1}$) which adds weighted picture data surrounding the current pixel is obtained through the adder 109 during the time interval of outputting picture data D_{PRI} of the regions AR5 as picture data of the current pixel.

A multiplier 110 doubles the picture data $A_{0,0}$ of the current pixel, and then adds the resulting data to output data D_H of the adder 109 at an adder 111.

A divider 112 divides output data D_{H0} of the adder 111 to $1/16$, and outputs the resulting data D_{PRO} to the arithmetic and logic circuit 97 (FIG. 16).

Thus, during the time period in which the picture data D_{PRI} of the regions AR1, AR3, AR7 and AR9 of the four corners of the data block DB are outputted as picture data of the current pixel, picture data $16A_{0,0}$ of the current pixel which has been weighted 16 times through the adder 111 is obtained (FIG. 17), and is then divided by the divider 112 to output the picture data $A_{0,0}$ of the current pixel.

When each picture data $A_{1,1}$ to $A_{1,-1}$ is arranged to correspond to FIG. 19 as showing in FIGS. 21 and 22, 3×3 output data of two dimensional filter circuit in which only $A_{0,0}$ is weighted with a value of 1 can be obtained.

During a time interval in which the picture data D_{PRI} of the regions AR2 and AR8 are outputted as picture

data of the current pixel, addition data $(4A_{1,0} + 8A_{0,0} + 4A_{1,0})$ can be obtained by weight adding picture data $A_{1,0}$, $A_{0,0}$ and $A_{1,0}$ of the next, the current and the previous pixels, and can thus be divided by the divider 112 to produce picture data $(A_{1,0} + 2A_{0,0} + A_{1,0})/4$.

Thus, normalized 3 x 3 output data of the two dimensional filter circuit can be obtained by weight adding picture data of three horizontally consecutive pixels with values 1, 2 and 1.

During the time interval in which the picture data D_{PR1} of the regions AR4 and AR6 are outputted as the picture data of the current pixel, addition data $(4A_{0,-1} + 8A_{0,0} + 4A_{0,1})$ having the picture data $A_{0,-1} + A_{0,0} + A_{0,1}$ of the next, the current and the previous line weight added is obtained, and is thus divided by the divider 112 to produce picture data $(A_{0,-1} + 2A_{0,0} + A_{0,1})/4$.

Thus, normalized 3 x 3 output data of the two dimensional filter circuit can be obtained by weight adding picture data of three vertically consecutive pixels with values 1, 2 and 1.

During the time interval in which the picture data D_{PR1} of the region AR5 is outputted as the picture data of the current pixel, addition data $(A_{1,-1} + 2A_{1,0} + A_{1,1} + 2A_{0,-1} + 4A_{0,0} + 2A_{0,1} + A_{1,-1} + 2A_{1,0} + A_{1,1})$ having the picture data $A_{1,-1}$ to $A_{1,1}$ weight added is obtained, and is thus divided by the divider 112 to produce picture data $(A_{1,-1} + 2A_{1,0} + A_{1,1} + 2A_{0,-1} + 4A_{0,0} + 2A_{0,1} + A_{1,-1} + 2A_{1,0} + A_{1,1})/16$.

Thus, normalized 3 x 3 output data of the two dimensional filter circuit can be obtained by sequentially weight adding picture data of nine vertically and horizontally consecutive pixels.

More specifically, a filter circuit with a characteristic defined by the following equation can be obtained by switching contacts of the selection circuits 102A, 102B, 108A and 108B

$$F = \frac{1}{(a+2)(b+2)} \cdot \begin{vmatrix} 1 & a & 1 \\ b & ab & b \\ 1 & a & 1 \end{vmatrix} \cdots (6)$$

where multipliers of the multipliers 105 and 110 are a and b, and the divisor c of the divider 96 is expressed as $(a+2)(b+2)$.

The characteristics of the loop filter circuit 98 can be changed by switching contacts of the selection circuits 102A, 102B, 108A and 108B depending on the position of the picture data D_{PR1} within the data block.

Thus, there is no need to use several kinds of filter circuits, and boundaries between data blocks can be made unobtrusive with a simple construction as a whole.

In this embodiment, the vertical digital filter circuit which outputs picture data consecutive in the vertical scanning direction from each of the delay circuits 101A and 101B is built by connecting the delay circuits 101A and 101B in series whereas the selection circuits 102A and 102B and the adder 104 constitute a vertical selection circuit which selectively outputs picture data outputted from the vertical digital filter circuit.

On the other hand, the horizontal digital filter circuit which outputs picture data consecutive in the horizontal scanning direction from each of the delay circuits 107A, 107B and 107C is built by connecting the delay circuits 107A, 107B and 107C in series whereas the selection circuits 108A and 108B and the adder 109 constitute a horizontal selection circuit which selectively outputs picture data outputted from the horizontal digital filter circuit.

Furthermore, picture data D_{PRO} can be outputted in the order of inputted picture data by building the loop filter circuit 98 in this manner, and thereby the construction of the input/output circuit of the loop filter circuit 98 can be simplified.

In FIG. 16 square circuits 121, 122 and 123 output squares of picture data D_{IND} , differential data D_z and differential data D_{Fz} , respectively.

Arithmetic and logic unit 124, 125, 126 and 127 add picture data D_{IND} and output data of the squares circuits 121, 122 and 123 to output data of latch circuits 128, 129, 130 and 131, respectively, and outputs results of

the summing to latch circuits 128, 129, 130 and 131.

Thus, the arithmetic and logic circuits 124, 125, 126 and 127 detect evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} , defined by the following equations, for each macro block:

$$D_{H1} = \Sigma (A) \quad (7)$$

$$D_{H2} = \Sigma (A)^2 \quad (8)$$

$$D_{H3} = \Sigma (A - B)^2 \quad (9)$$

$$D_{H4} = \Sigma (A - FB)^2 \quad (10)$$

where A and B represents picture data D_{IND} and picture data D_{PRI} and FB is the value of the output data D_{PRO} of the loop filter circuit 98. The evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} are outputted to a digital signal processing circuit 132.

The digital signal processing circuit 132 adds evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} to header D_{HET} outputted from the motion vector detection circuit 68, and outputs the resulting data to a digital signal processing circuit 134 through a buffer memory circuit 135.

The digital signal processing circuit 134 is constituted by an operation processing circuit similarly with the digital signal processing circuit 132, and controls to switch the switch circuit 91 and the switch circuit 95 according to the header D_{HET} .

More specifically, picture data D_{IND} is outputted to the subsequent discrete cosine transform circuit 71 for every predetermined frames according to the number of frame of the header D_{HET} .

Thus, in the video signal transmission system video signals can be transmitted by intra coding every predetermined frames.

On the other hand, differential data D_{FZ} is outputted to the discrete cosine transform circuit 71 for the remaining frames, and video signals inter coded are transmitted.

In this event, the digital signal processing circuit 134 obtains results of comparison between the evaluation data D_{H2} , D_{H3} and D_{H4} and outputs picture data D_{IND} to the discrete cosine transform circuit 71 in place of differential data D_{FZ} when the evaluation data D_{H2} is smaller than evaluation data D_{H3} and D_{H4} .

More specifically, when the evaluation data D_{H2} is smaller than evaluation data D_{H3} and D_{H4} according to the equations (8) to (10), picture data can be efficiently sent by transmitting picture data D_{IND} in place of differential data D_{FZ} .

Moreover, the digital signal processing circuit 134 outputs differential data D_Z to the discrete cosine transform circuit 71 in place of differential data D_{FZ} when the evaluation data D_{H4} is smaller than evaluation data D_{H2} and D_{H3} .

That is, there is a case where boundaries between data blocks are unobtrusive event if differential data D_Z is coded, and there is another case where efficient transmission is performed by coding differential data D_Z for differential data D_{FZ} .

Thus, as in this embodiment, video signals can be transmitted efficiently as a whole by switching the coding operation according to evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} .

Furthermore, the digital signal processing circuit 134 removes evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} from the header D_{HET} outputted from the digital signal processing circuit 132, and then adds information to switch the switch circuits 91 and 95 to renew the header D_{HET} . The header D_{HET} renewed is outputted through the buffer memory circuit 136 to the discrete cosine transform circuit 71.

(6-3) Decoder circuit

As shown in FIG. 23, the decoder circuit 69 provides the picture data D_{INV} and D_Z and the header D_{HET} outputted from the inverse discrete cosine transform circuit 75 to an adder 141 and a header detection circuit 142.

The header detection circuit 142 separates a frame number, address data of a block group, macro block and data blocks, and a motion vector from the header D_{HET} for outputting to address data producing circuits 143 and 145.

The address data producing circuits 143 and 145 generate address data for writing to frame memory circuits 146, 147 and 148, and at the same time produce address data for reading the frame memory circuit 146 according to the motion vector.

The header detection circuit 142 outputs identification data for inter and intra coding to a mode indication circuit 149 as well as switch signals SEL5 and SEL6 according to the identification data for inter and intra coding and according to on-off information of the loop filter circuit.

Thus, the header detection circuit 142 switches contacts of the selection circuits 150 and 151, and switches the operation of the decoder circuit 69 in accordance with picture data D_{INV} and D_Z reconstructed in the inverse discrete cosine transform circuit 75.

More specifically, in a case where picture data D_{INV} intra coded is processed, the header detection circuit 142 performs selective control of the earth contact of the selection circuit 150.

Thus, the picture data D_{INV} reconstructed in the inverse discrete cosine transform circuit 75 is outputted through the adder 141 and a clipping circuit 152, and is stored in the frame memory circuits 146, 147 and 148 according to address data outputted from the write address data producing circuit 143.

In a case where differential data D_z inter coded selective control of the selection circuit 151 side contact of the selection circuit 150.

This enables picture data outputted at a timing lagging by a motion vector from the frame memory circuit 146 through a loop filter circuit 153 or a register circuit 154.

Thus, the differential data D_z reconstructed in the inverse discrete cosine transform circuit 75 is constituted by an operation processing circuit, and is actuated based on reference signals outputted from a control circuit 133 synchronously with a system clock signal S_{CK} .

Furthermore, the digital signal processing circuit 132 adds evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} to header D_{HET} outputted from the motion vector detection circuit 68, and outputs the resulting data to a digital signal processing circuit 134 through a buffer memory circuit 135.

The digital signal processing circuit 134 is constituted by an operation processing circuit similarly with the digital signal processing circuit 132, and controls to switch the switch circuit 91 and the switch circuit 95 according to the header D_{HET} .

More specifically, picture data D_{IND} is outputted to the subsequent discrete cosine transform circuit 71 for every predetermined frames according to the number of frame of the header D_{HET} .

Thus, in the video signal transmission system video signals can be transmitted by intra coding every predetermined frames.

On the other hand, differential data D_{FZ} is outputted to the discrete cosine transform circuit 71 for the remaining frames, and video signals inter coded are transmitted.

In this event, the digital signal processing circuit 134 obtains results of comparison between the evaluation data D_{H2} , D_{H3} and D_{H4} and outputs picture data D_{IND} to the discrete cosine transform circuit 71 in place of differential data D_{FZ} when the evaluation data D_{H2} is smaller than evaluation data D_{H3} and D_{H4} .

More specifically, when the evaluation data D_{H2} is smaller than evaluation data D_{H3} and D_{H4} according to the equations (8) to (10), picture data can be efficiently sent by transmitting picture data D_{IND} in place of differential data D_{FZ} .

Moreover, the digital signal processing circuit 134 outputs differential data D_z to the discrete cosine transform circuit 71 in place of differential data D_{FZ} when the evaluation data D_{H4} is smaller than evaluation data D_{H2} and D_{H3} .

That is, there is a case where boundaries between data blocks are unobtrusive even if differential data D_z is coded, and there is another case where efficient transmission is performed by coding differential data D_z for differential data D_{FZ} .

Thus, as in this embodiment, video signals can be transmitted efficiently as a whole by switching the coding operation according to evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} .

Furthermore, the digital signal processing circuit 134 removes evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} from the header D_{HET} outputted from the digital signal processing circuit 132, and then adds information to switch the switch circuits 91 and 95 to renew the header D_{HET} . The header D_{HET} renewed is outputted through the buffer memory circuit 136 to the discrete cosine transform circuit 71.

(6-3) Decoder circuit

As shown in FIG. 23, the decoder circuit 69 provides the picture data D_{INV} and D_z and the header D_{HET} outputted from the inverse discrete cosine transform circuit 75 to an adder 141 and a header detection circuit 142.

The header detection circuit 142 separates a frame number, address data of a block group, macro block and data block, and a motion vector from the header D_{HET} for outputting to address data producing circuits 143 and 145.

The address data producing circuits 143 and 145 generate address data for writing to frame memory circuits 146, 147 and 148, and at the same time produce address data for reading the frame memory circuit 146 according to the motion vector.

The header detection circuit 142 outputs identification data for inter and intra coding to a mode indication circuit 149 as well as switch signals $SEL5$ and $SEL6$ according to the identification data for inter and intra coding and according to on-off information of the loop filter circuit.

Thus, the header detection circuit 142 switches contacts of the selection circuits 150 and 151, and switches the operation of the decoder circuit 69 in accordance with picture data D_{INV} and D_z reconstructed in the inverse discrete cosine transform circuit 75.

More specifically, in a case where picture data D_{INV} intra coded is processed, the header detection circuit 142 performs selective control of the switch contact of the selection circuit 150.

Thus, the picture data D_{INV} reconstructed in the inverse discrete cosine transform circuit 75 is outputted through the adder 141 and a clipping circuit 152, and is stored in the frame memory circuits 146, 147 and 148 according to address data outputted from the write address data producing circuit 143.

In a case where differential data D_z inter coded is processed, the header detection circuit 142 makes a selective control of the selection circuit 151 side contact of the selection circuit 150.

This enables picture data outputted at a timing lagging by a motion vector from the frame memory circuit 146 through a loop filter circuit 153 or a register circuit 154.

Thus, the differential data D_z reconstructed in the inverse discrete cosine transform circuit 75 is added to the picture data shifted by the motion vector and read from the frame memory circuit 146 at the adder 141, and is then stored in the frame memory circuits 146, 147 and 148 to thereby reconstruct the original picture data.

In a case where the loop filter circuit 98 is selected in the differential data producing circuit 70 (FIG. 16), the selection circuit 151 is controlled so that the loop filter circuit 135 side contact is selected in reconstructing corresponding picture data, and thereby the original picture data is reconstructed with reference to the picture data of the previous frame of which high frequency band has been suppressed similarly with the case of producing the differential data D_z .

Thus, differential data D_{FZ} which is constructed through the loop filter circuit 98 can be reconstructed through the loop filter circuit 153, and thereby boundaries between macro blocks can be made unobtrusive.

The loop filter circuit 153 is constituted by a two dimensional filter circuit of the same configuration as the loop filter circuit 98 (FIG. 17), and this enables characteristics of several kinds to be selected by merely switching contacts of the selection circuits. Thus, the construction of the decoder circuit 69 is simplified.

The frame memory circuit 147 temporarily stores reconstructed picture data by sequentially storing the picture data obtained through the adder 141, and then outputs picture data D_{SV} to the motion vector detection circuit 68 in the unit of a block group according to the address data outputted from the motion vector detection circuit 68.

This enables the motion vector detection circuit 68 to sequentially detect motion vectors according to the picture data D_{SV} reconstructed.

The frame memory circuit 148 selectively accepts picture data, obtained through the adder 141, and output data from the mode indication circuit 149 through the selection circuit 155, and outputs the data read in to a display 156.

The mode indication circuit 149 outputs picture data of different chrominance signals depending on intra coding and inter coding operations.

The selection circuit 155 outputs data concerning chrominance signals outputted from the mode indication circuit 149 to frame memory circuit 148 as well as picture data about luminance signals among picture data, outputted from the adder 141, from the frame memory circuit 148 when a predetermined actuator is operated on.

This enables the display 156 to display pictures different in color depending on intra coding and inter coding operations.

Thus, at the end of the transmitter maintenance workers can confirm by visual observation pictures to be reconstructed at the destination. This enables the operation of the video signal transmission system 65 to be confirmed. In this event, it is possible to confirm according to differences in display colors whether intra coding or inter coding is performed.

As shown in FIG. 24, in which each of corresponding parts of FIG. 10 are designated by the same reference numeral, in a decoder circuit 86 the frame memory circuit 147 is omitted and the output data of the frame memory circuit 148 is outputted to the video signal processing circuit 87.

This enables pictures sent from the destination to be monitored by the monitor 88 (FIG. 15), and further it is possible to confirm by turning on the predetermined actuator according to a need whether intra coding or inter coding operation is performed at the destination.

Thus, also in the decoder circuit 86 the overall construction can be simplified by using a loop filter circuit 153 of the same configuration as the differential data producing circuit 70.

In a case where loop filter circuits are used in this type of the video signal transmission system, three loop filter circuits with the same characteristic are needed, and hence when individual loop filter circuits are complicated in construction, then the video signal transmission system as a whole becomes large-sized.

However, if as in this embodiment, a loop filter circuit which is capable of selecting several kinds of characteristics by switching contacts of the selection circuits, the video signal transmission system 65 (FIG. 15) as a whole can be simplified with ease.

(6-4) Operation of the third embodiment

In the construction above, video signals S_V outputted from the television camera 66 (FIG. 15) undergoes the preliminary processing in the video signal processing circuit 67 to reduce the amount of data and are con-

verted picture data D_{IN} of the CCITT format.

A motion vector of picture data D_{IN} is detected for every macro block after the array of the picture data is rearranged in the motion vector detection circuit 16.

Here, picture data D_{PRI} for comparison reference is produced according to the detected motion vector, and the picture data D_{PRI} is outputted to the differential data construction circuit 70 together with the picture data D_{IND} (FIG. 16).

In the differential data producing circuit 70, differential data D_z is produced by directly subtracting the picture data D_{PRI} from the picture data D_{IND} .

Simultaneously, in the loop filter circuit 98 (FIG. 17) the picture data D_{PRI} is fed to the delay circuits 101A and 101B, and thereby picture data of the previous, current and next lines are produced.

The picture data of the previous, current and next lines are selectively outputted through the selection circuits 102A and 102B according to the picture data of the current line, and then added in the adder 104, after which the resulting data is added to the weighted picture data of the current line in the adder 106.

This provides picture data D_{VO} in the vertical scanning direction with frequency characteristic according to selective outputs of the selection circuits 102A and 102B.

The picture data D_{VO} is fed to the delay circuits 107A, 107B and 107C, where picture data of previous, current and next pixels are constructed.

The picture data of the previous, current and next pixels are selectively outputted through the selection circuit 108A and 108B according to the picture data of the current pixel to undergo addition in the adder 109, and are then added to weighted picture data of the current pixel at the adder 111.

This enables picture data D_{PRO} to be provided in the horizontal scanning direction with frequency characteristic depending on selective outputs of the selection circuits 108A and 108B.

The picture data D_{PRO} of the loop filter circuit 98 is subtracted from the picture data D_{IND} to produce differential data D_{FZ} .

The evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} of the equations (7) to (10) are detected from the picture data D_{IND} , and the differential data D_z and differential data D_{FZ} in the arithmetic and logic unit 124 to 127, and the picture data D_{IND} and the differential data D_z and D_{FZ} are selectively outputted to the subsequent discrete cosine transform circuit 71 (FIG. 15) according to evaluation data D_{H1} , D_{H2} , D_{H3} and D_{H4} .

In this manner, in the frames inter coded differential data D_z and D_{FZ} are outputted to the discrete cosine transform circuit 71 whereas in the frame intra coded picture data D_{IND} is directly outputted to the discrete cosine transform circuit 71.

The transformed data D_{DCT} which has been obtained through the discrete cosine transform circuit 71 is quantized in the quantizer 72, and then undergoes the variable length coding processing in the variable length coding circuit 76 through the buffer circuit 77. The output data is sequentially sent to the destination through the transmission buffer circuit 73, the stuff bit adding circuit 78, the error correction circuit 79 and the multiplex conversion circuit 80.

The output data of the quantizer 72 is decoded in the decoder circuit 69 to picture data through the inverse quantization circuit 74 and the inverse discrete cosine transform circuit 75, and the picture data is outputted as picture data D_{SV} of the previous frame for detecting the motion vector.

When the differential data D_{FZ} which is produced through the loop filter circuit 98 is processed in this event, picture data of the previous frame outputted from the frame memory circuit 146 (FIG. 24) is added to differential data D_{FZ} through the loop filter circuit 153, and thereby boundaries between data blocks are made less obtrusive.

(6-5) Effects of the embodiment

According to the foregoing construction, it is possible that picture data of previous, current and next lines are selectively outputted, and that the selective output is switched by selectively outputting the picture data of the previous, current and next lines to thereby switch the characteristic of the loop filter circuit with a simple construction.

(7) Modifications of the third embodiment

(7-1) In the embodiment above described, it is stated that the characteristic of the loop filter circuit is switched as shown in FIG. 22. However, the present invention is not limited to this. If the contacts P1 and P2 are selected as shown in FIG. 25, for example, a filter characteristic as shown in FIG. 26 is obtained, and hence the present invention is widely applied to cases to obtain various characteristics according to needs.

(7-2) Moreover, in the above embodiment, the case where picture data of a current line and a current pixel are added to the addition data of the adders 104 and 109 with weights is described but the present invention is not limited to this. The addition operation may be omitted according to needs.

(7-3) Furthermore, in the above embodiment, the case is stated in which after a characteristic is set in the vertical scanning direction, a horizontal scanning direction characteristic is set, but the present invention is not restricted to this. The picture data D_{PRI} may be inputted to the delay circuit 107A, the output data of the adder 111 may be outputted to the delay circuit 101A, and the output data of the adder 106 may be divided by the divider 112.

(7-4) In the foregoing embodiment, it is stated that the present invention is applied to the video signal transmission system for transmitting video signals together with voice signals but the present invention is not limited to this. The present invention may be widely applied to cases such as a case of transmitting video signals high efficiency coded and a case of saving a recording media. The present invention may be further applied to a two dimensional filter circuit to correct picture data in frequency characteristic.

(8) The fourth embodiment

(8-1) Construction of the fourth embodiment

In FIG. 27, 161 generally designates a picture phone system, which outputs video signal S_V and voice signal S_A to a destination through the line L1.

In addition, the picture phone 161 demodulates data transmitted from the destination through the line L1 to output video signal S_{VOUT} and voice output signals S_{AOUT} .

For this purpose, the line connecting unit 162 performs a line connecting operation to interconnect between the destination and the line L1.

More specifically, when the line L1 is connected to a predetermined destination after a calling signal is outputted to the line L1, the line connecting unit 162 detects a answer signal, so that the logic level of the control signals S_{CONT} rises.

Moreover, the line connecting unit 162 cuts off the line L1 by outputting an on-hook signal after the conversation is completed.

On the other hand, a video signal transmission system 163 performs a coding operation of the video signal S_V by converting the video signals S_V to digital signals in a transmitter 163A, and then outputs the signals by multiplexing with digital voice signals. In this manner, pictures and voices of the speaker are outputted to the destination through the line connecting unit 162.

In the coding operation by converting the video signals S_V to digital signals, the video signal transmission system 163, as shown in FIG. 28, selects the intra coding operation to process picture data for a predetermined time interval T after the control signals S_{CONT} rises.

After the lapse of the time interval T, picture data of every predetermined frames undergoes the intra coding operation and is then transmitted.

In this manner, it is possible to intra code and send several frames of picture data immediately after connection of the line L1.

It is thus possible to monitor a picture of the speaker at the end of the video signal transmission system 163 just after the connection of the line L1, and hence natural communication is realized.

Accordingly, it is possible to enhance facility of the video signal transmission system 163.

Moreover, in the video signal transmission system 163, output data of the line connecting unit 162 is decoded in a receiver 163B, and then outputs video signal S_{VOUT} and voice output signals S_{AOUT} . In this manner, conversation is achieved, monitoring pictures of the speaker.

The video signal transmission system 163, as described in FIG. 15, takes a picture of a speaker through a television camera 66, and the video signals S_V outputted from the television camera 66 are provided to a video signal processing circuit 67.

(8-2) Operation of the fourth embodiment

In the construction above, video signals S_V outputted from the television camera 66 undergoes the preliminary processing in the video signal processing circuit 67 to reduce the amount of data and are converted to picture data D_{IN} of the CCITT format.

A motion vector of picture data D_{IN} is detected for every macro block after the array of the picture data is rearranged in the motion vector detection circuit 68.

Here, picture data D_{PRI} for comparison reference is produced according to the detected motion vector, and the picture data D_{PRI} is outputted to the differential data construction circuit 70 together with the picture data D_{IND} .

In the differential data construction circuit 70, the intra coding operation is selected at a predetermined frame cycle, and in this event picture data D_{IND} is directly outputted to the discrete cosine transform circuit 71.

On the other hand, in the inter coding picture data D_{PRI} is subtracted from picture data D_{IND} to produce differential data D_z and D_{Fz} , which are outputted to the discrete cosine transform circuit 71.

When in this event the line L1 is connected and the logic level of the control signals S_{CONT} rises, picture

data D_{IND} of frames are outputted to the discrete cosine transform circuit 71 by control switching of the switch circuit 91 by the digital signal processing circuit 134 (FIG. 16).

Thus, the intra frame operation is selected, and at the destination conversation may be had without unusualness, monitoring pictures of speaker just after the line L1 is connected.

5 The transformed data D_{DCT} which has been obtained through the discrete cosine transform circuit 71 is quantized in the quantizer 72, and then undergoes the variable length coding processing in the variable length coding circuit 76 through the buffer circuit 77. The output data is sequentially sent to the destination through the transmission buffer circuit 73, the stuff bit adding circuit 78, the error correction circuit 79 and the multiplex conversion circuit 80.

10 The output data of the quantizer 72 is decoded in the decoder circuit 69 to picture data through the inverse quantization circuit 74 and the inverse discrete cosine transform circuit 75, and the picture data is outputted as picture data D_{SV} of the previous frame for detecting the motion vector.

(8-3) Effects of the fourth embodiment

From the foregoing construction, picture data of several frames are intra coded and then sent just after the line L1 is connected, and thereby at the destination conversation may be had without unusualness, monitoring pictures of speaker just after the line L1 is connected. Thus, facility is improved compared to the prior art.

(8-4) Modification of the fourth embodiment

15 In the preceding embodiment, picture data of several frames are intra coded and then sent just after the line L1 is connected, and then switching is made to the normal operation. The present invention is not limited to this. For example, the operation may be switched to the intra frame coding just after the line L1 is cut off, and the connection of the line L1 may be waited for in the intra coding mode.

20 While there has been described in connection with the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention, and it is aimed, therefore, to cover in the appended claims all such changes and modifications as fall within the true spirit and scope of the invention.

Claims

- 30 1. A video signal coding method in which video signals are alternatively intra and inter coded and are then quantized for transforming to picture data, characterized in that:
the quantization is executed by enlarging the quantization step size to a predetermined rough quantization level when the picture data to be quantized is in an intra coded format.
- 35 2. A video signal coding system with a transmission buffer circuit, in which transmission picture data which has been high efficiency coded is temporarily stored in the transmission buffer circuit, and the transmission picture data stored is sequentially outputted to a transmission line according to a data transmission capacity of the transmission line, characterized in that:
the transmission picture data is frame dropped when an amount of residual data of the transmission
40 buffer circuit exceeds a predetermined upper limit; and
the frame dropping operation is completed when the amount of the residual data of the transmission buffer circuit reduces to a predetermined desired level smaller than the upper limit.
- 45 3. A filter circuit comprising:
a vertical digital filter circuit having a plurality of delay circuits connected in series, each delay circuit outputting picture data consecutive in the vertical scanning direction;
a vertical selection circuit for selectively outputting the picture data outputted from the vertical digital filter circuit;
a horizontal digital filter circuit having a plurality of delay circuits connected in series, each delay
50 circuit outputting picture data consecutive in the horizontal scanning direction; and
a horizontal selection circuit for selectively outputting the picture data outputted from the horizontal digital filter circuit; and wherein:
picture data are sequentially inputted to the vertical digital filter circuit or the horizontal digital filter circuit; the output data of the vertical selection circuit or the horizontal selection circuit is fed to the horizontal digital filter circuit or the vertical digital filter circuit; the picture data outputted from the horizontal selection circuit or the vertical selection circuit is corrected by switching the selective outputs from the vertical selection circuit and the horizontal selection circuit.
- 55

4. A video signal processing apparatus including a filter circuit according to claim 3.
5. A video signal transmission system in which video signals are transmitted by repeating inter coding and intra coding at a predetermined cycle, characterized in that:
5 the video signals of predetermined frames are intra coded and then transmitted after a line is connected to a destination.
6. A video signal coding method in which video signals are alternatively intra and inter coded and are then quantized for transforming to picture data, characterized in that:
10 a power of said picture data is calculated when said picture data to be quantized is a data inter coded, and then said quantization is executed with a quantization step size which is reduced data a predetermined ratio to a quantization step size of a previous frame when said power of picture data calculated is smaller than a predetermined threshold value.
- 15 7. A video signal coding method in which video signals are alternatively intra and inter coded and are then quantized for transforming to picture data, characterized in that:
 a power of said picture data is calculated when said picture data to be quantized is a data inter coded, and then said quantization is executed with a quantization step size which is enlarged to a predetermined
20 rough quantization step size value when said power of picture data calculated is larger than a predetermined threshold value.
- 25
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- 50
- 55

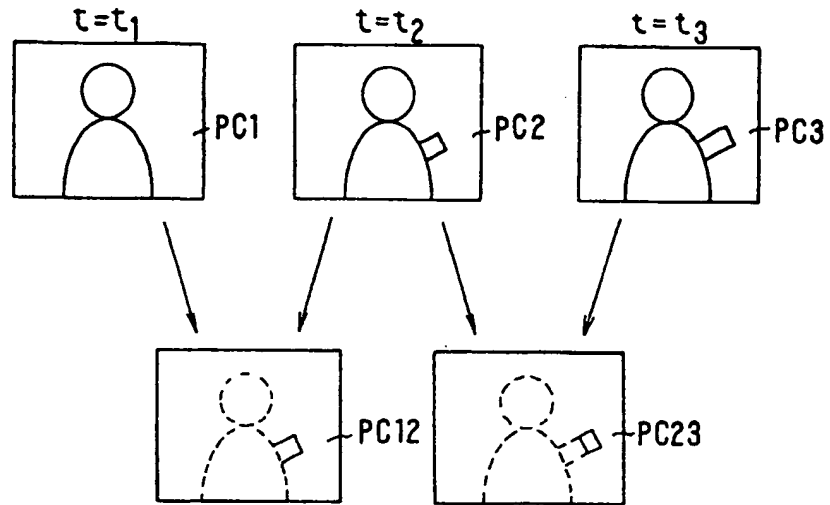


FIG.1 (PRIOR ART)

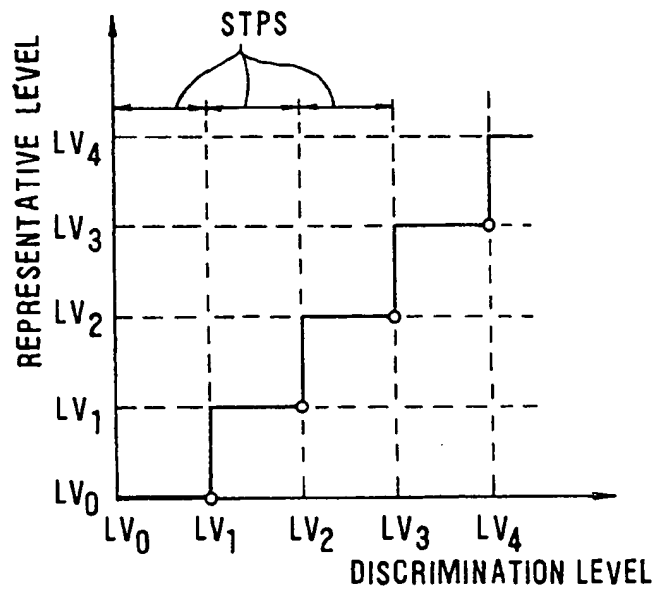


FIG.3 (PRIOR ART)

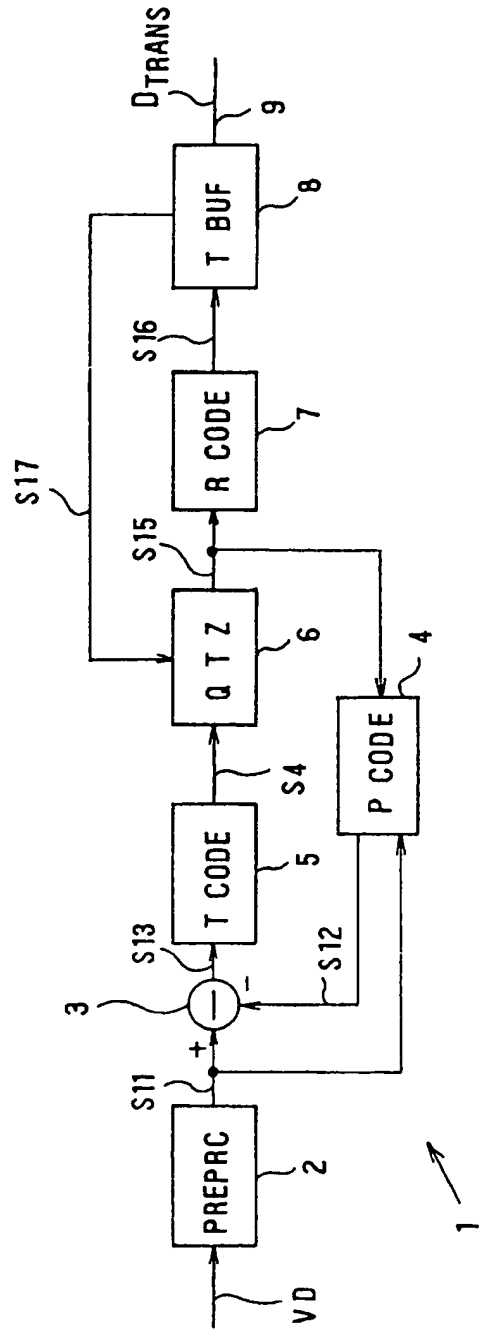


FIG. 2 (PRIOR ART)

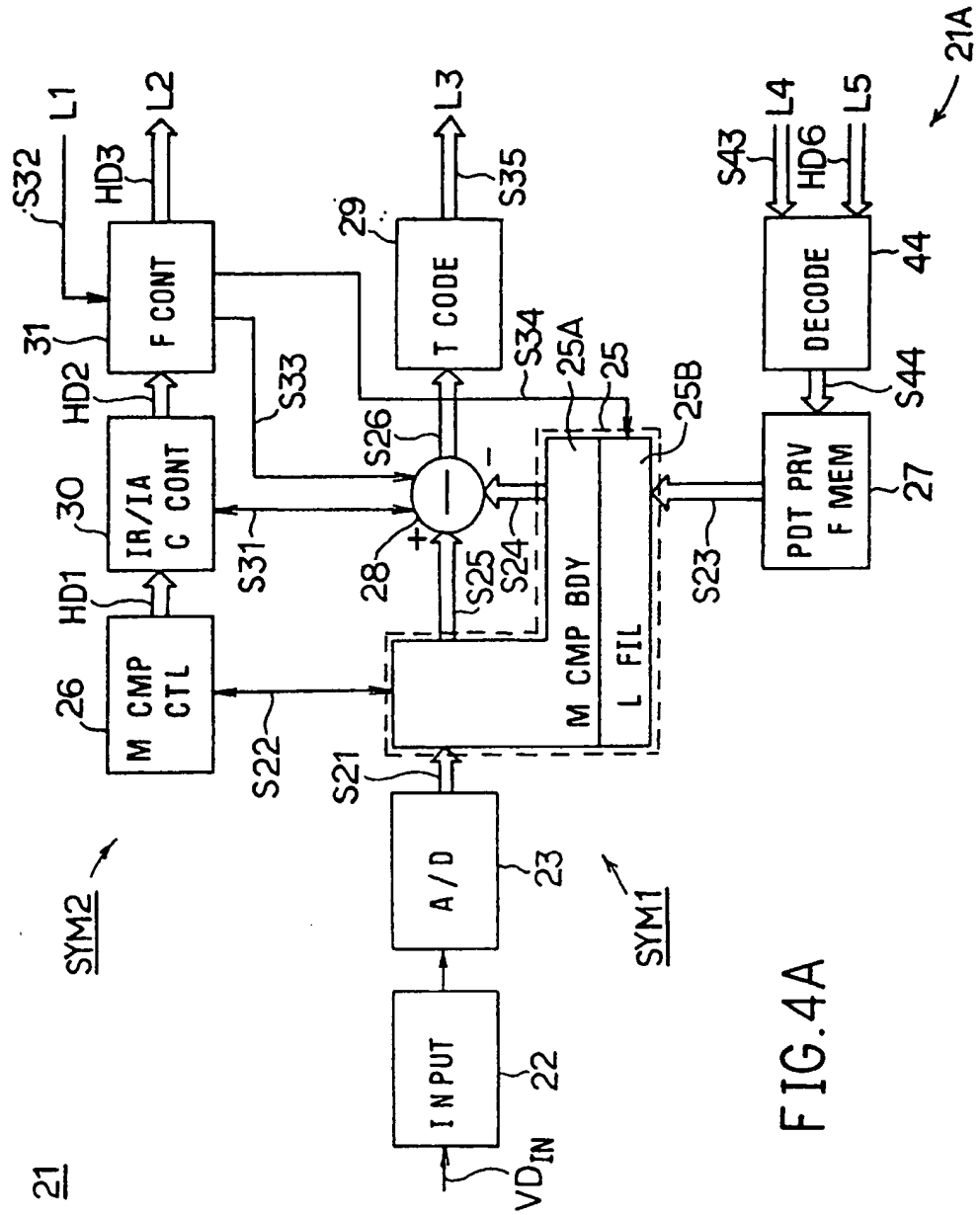


FIG. 4A

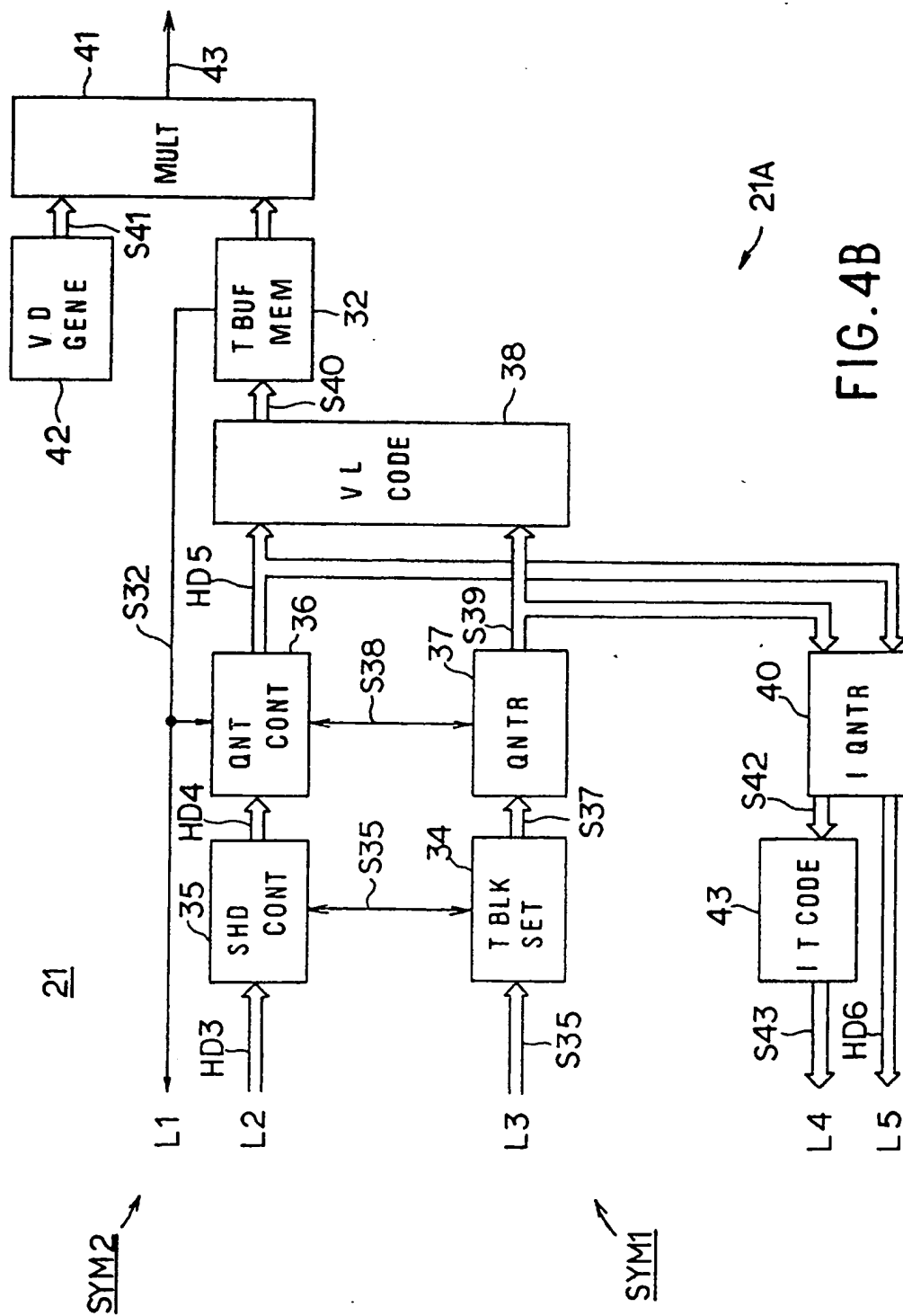


FIG. 4B

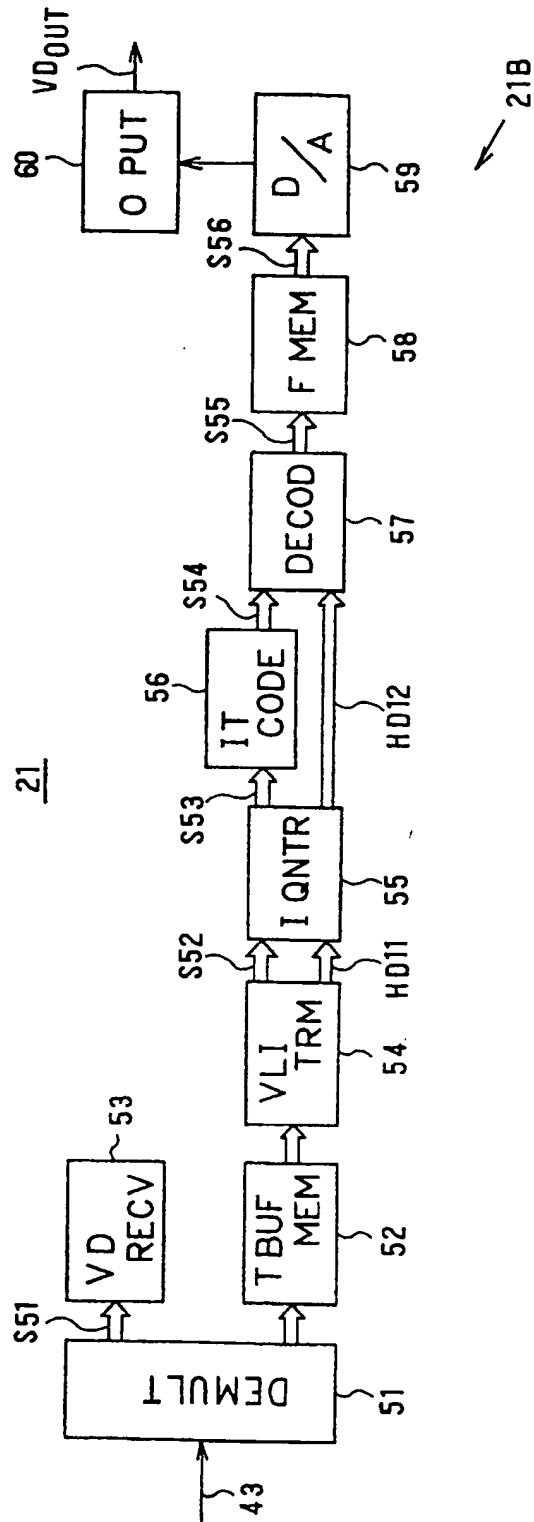


FIG. 5

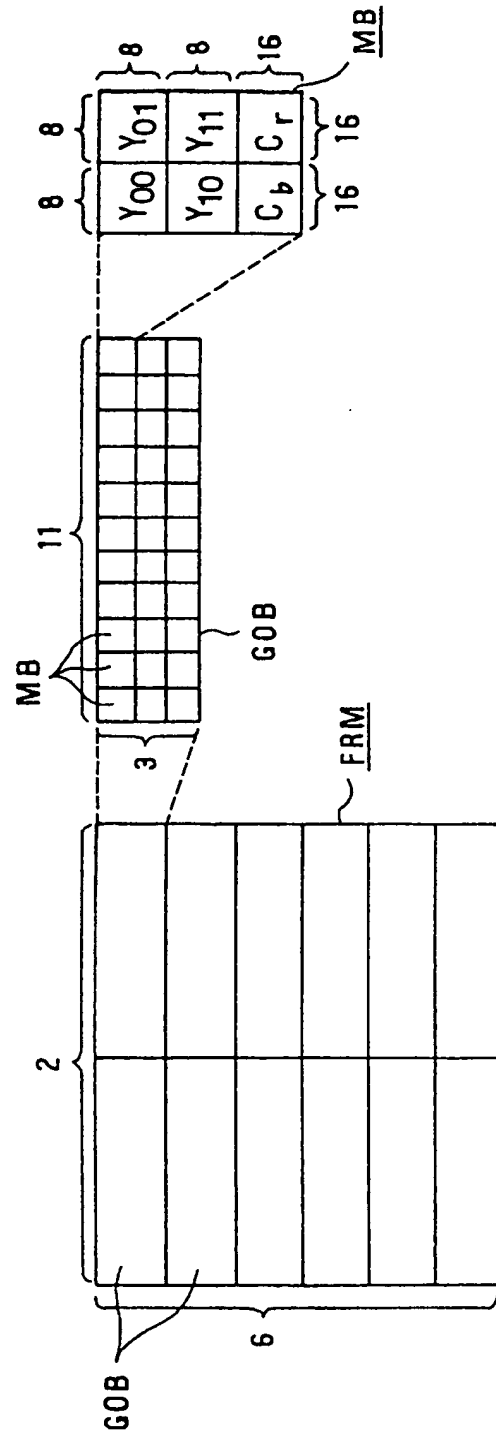


FIG. 6

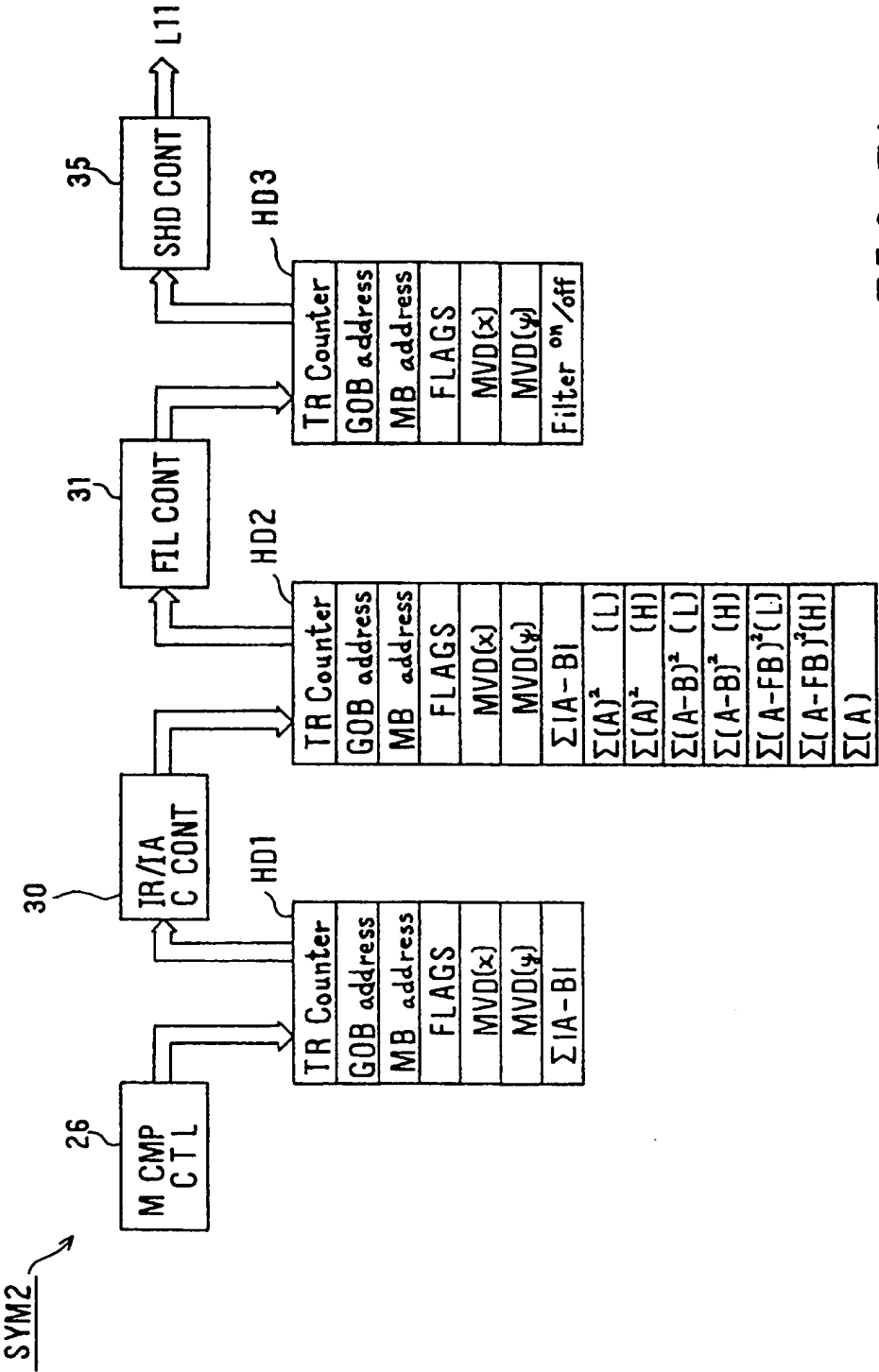
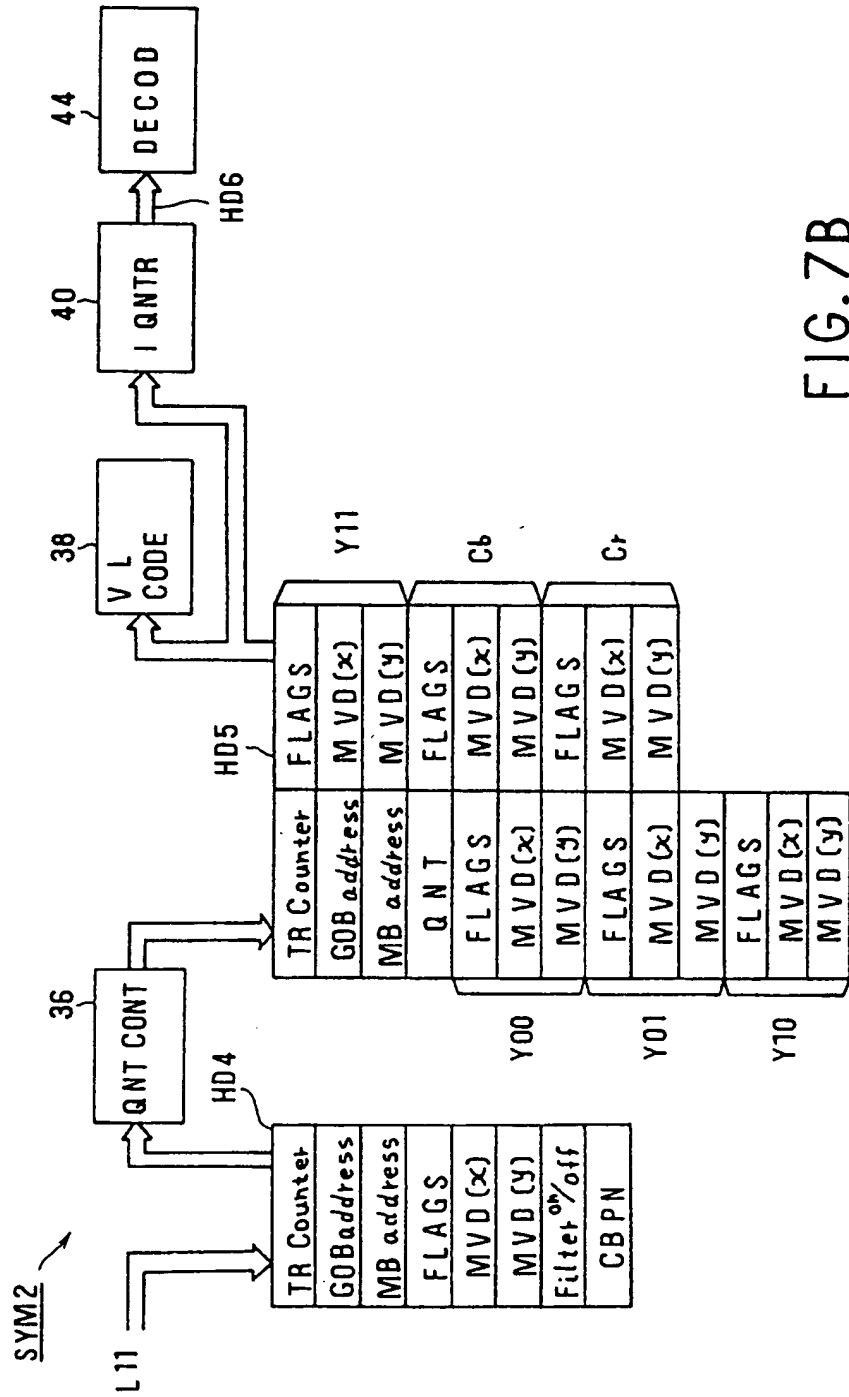


FIG. 7A



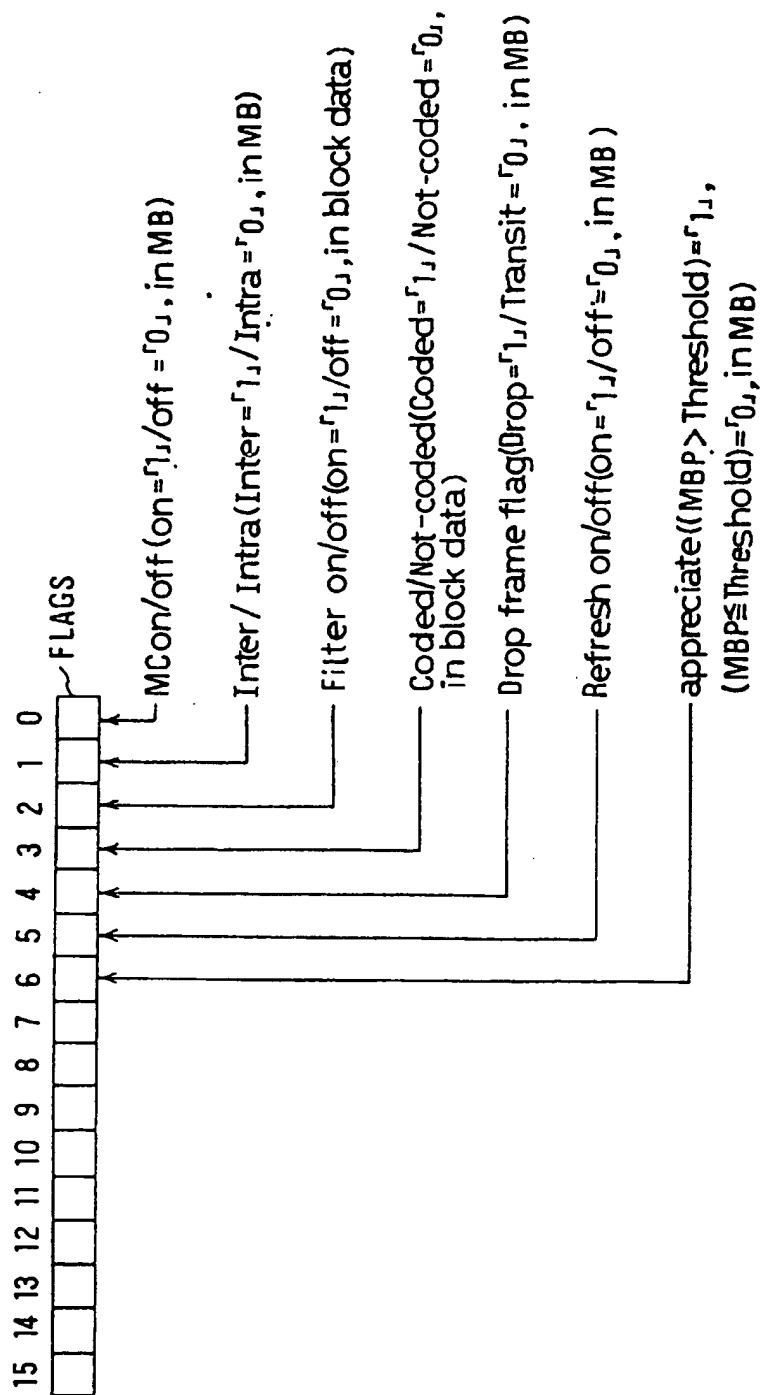


FIG. 8

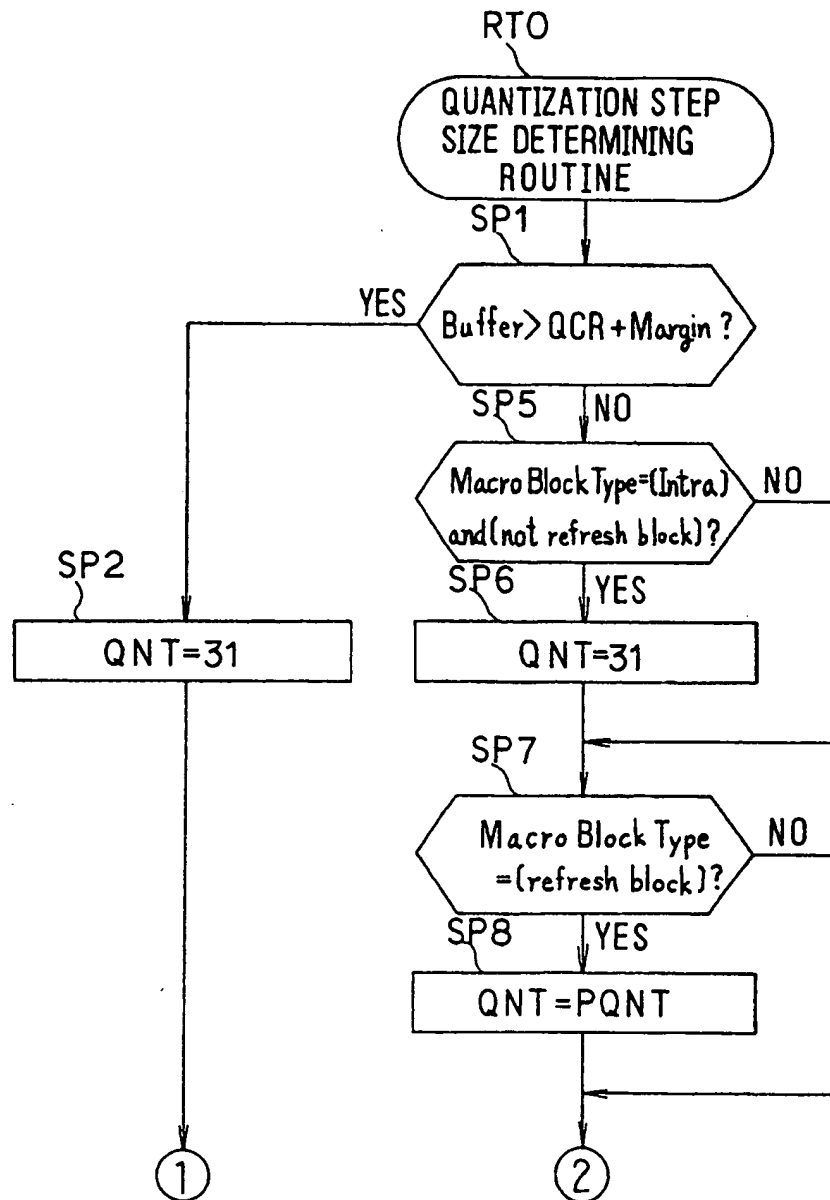


FIG.9A

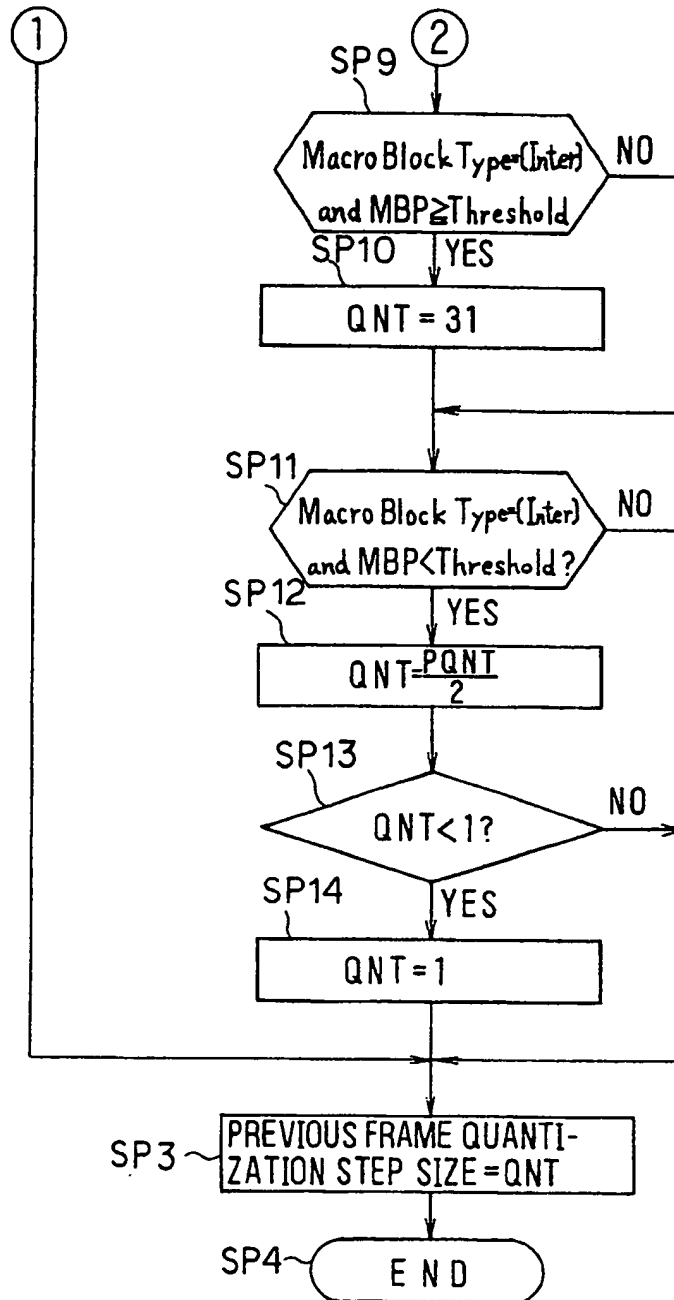


FIG. 9B

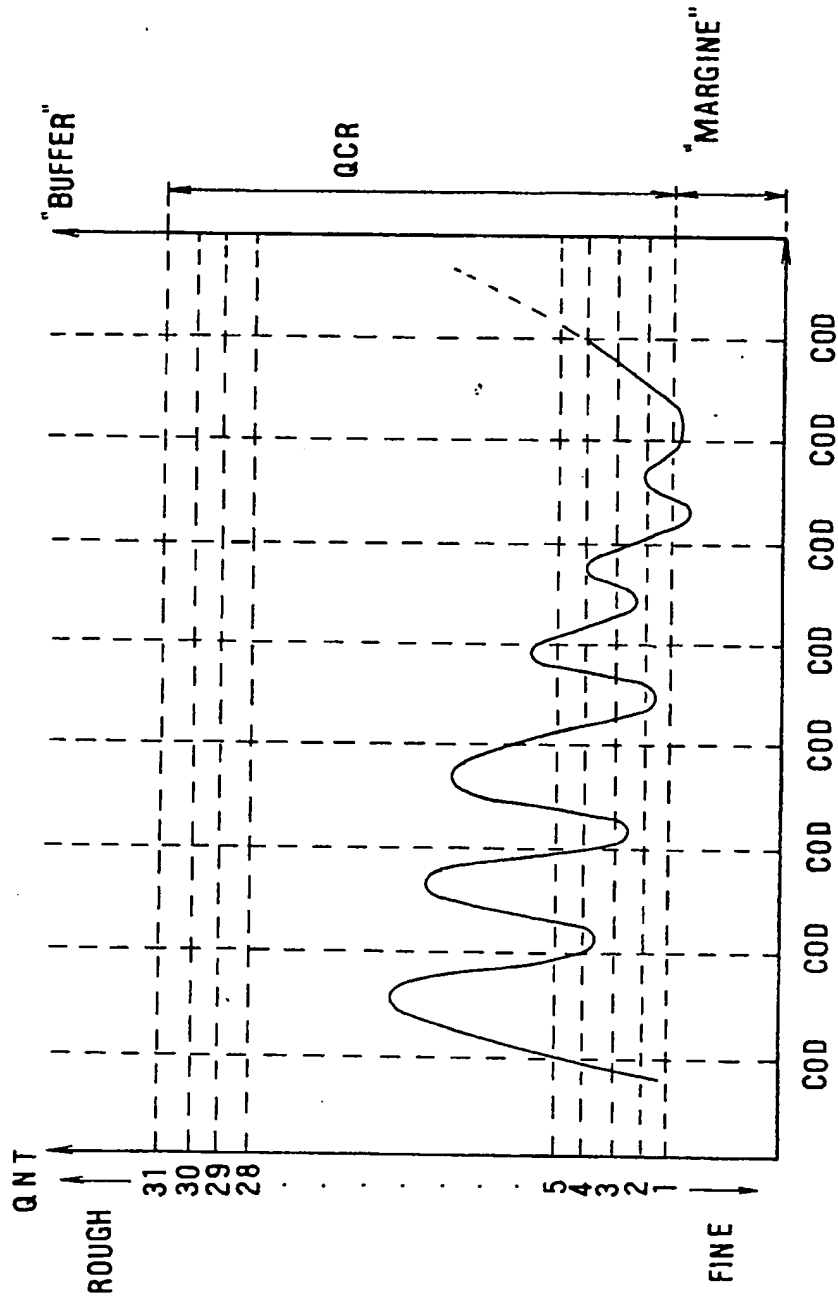


FIG.10

Bit 2	Bit 1	Bit 0	
Filter on/off (r'_{1J} =on, r'_{0J} =off)	Inter/Intra (r'_{1J} =Intra, r'_{0J} =Inter)	MC on/off (r'_{1J} =on, r'_{0J} =off)	Macro Block Type
0	1	0	Intra
0	0	0	Inter
0	0	1	MC-not filtered
1	0	1	MC-filtered

FIG.11

1	2	6	7	15	16	28	29
3	5	8	14	17	27	30	43
4	9	13	18	26	31	42	44
10	12	19	25	32	41	45	54
11	20	24	33	40	46	53	55
21	23	34	39	47	52	56	61
22	35	38	48	51	57	60	62
36	37	49	50	58	59	63	64

~ Coeff(i)
(i=1~64)

FIG.12

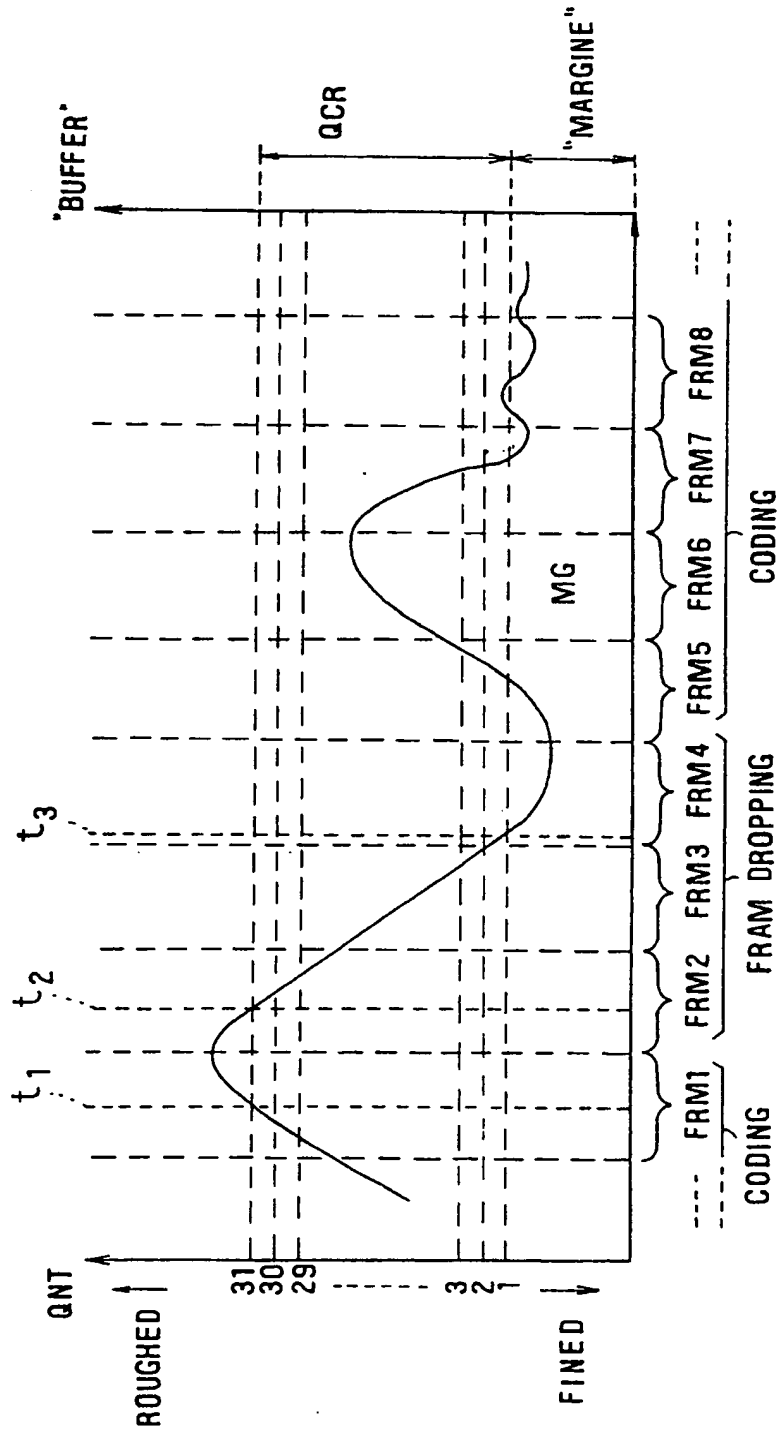


FIG.13

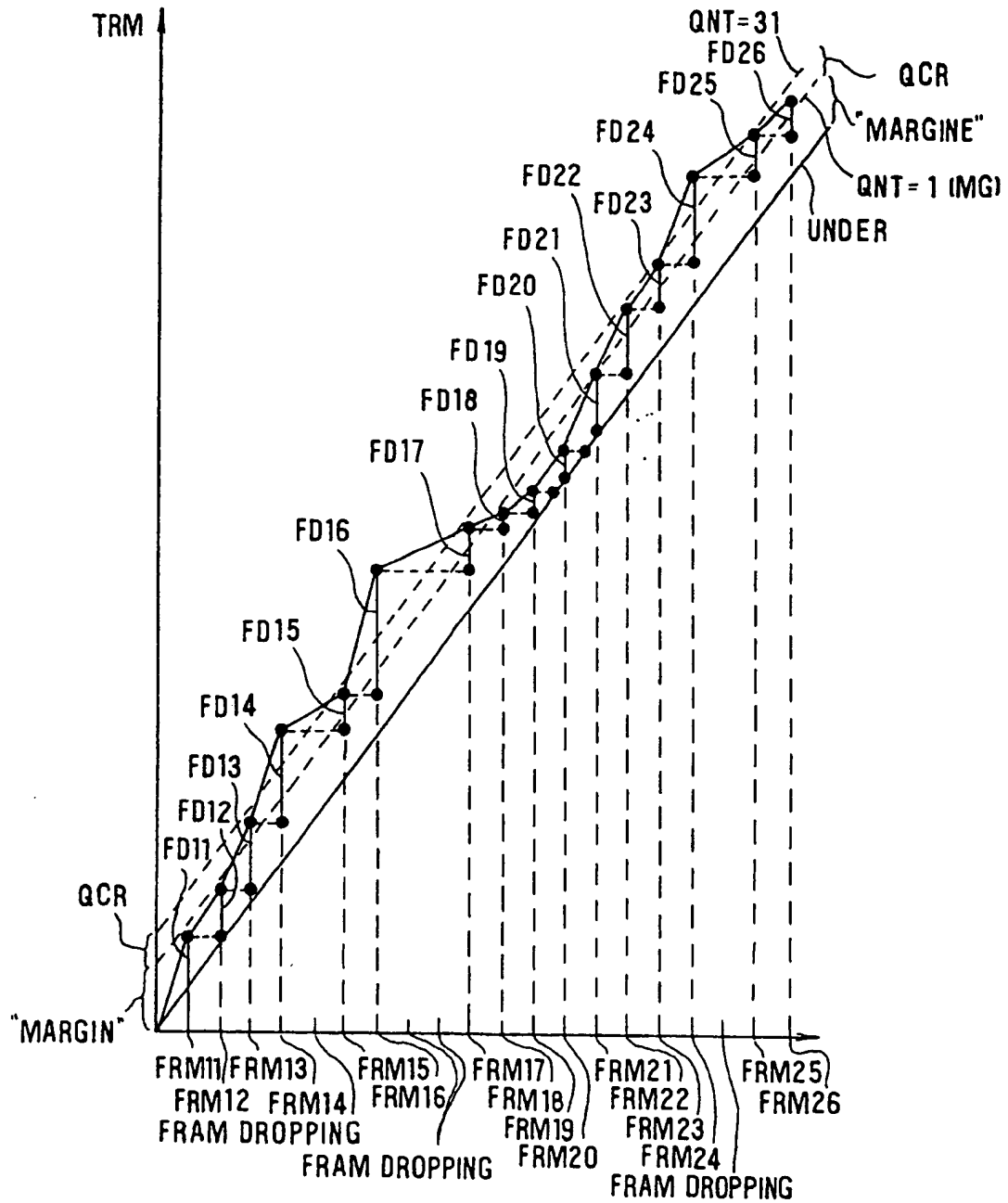
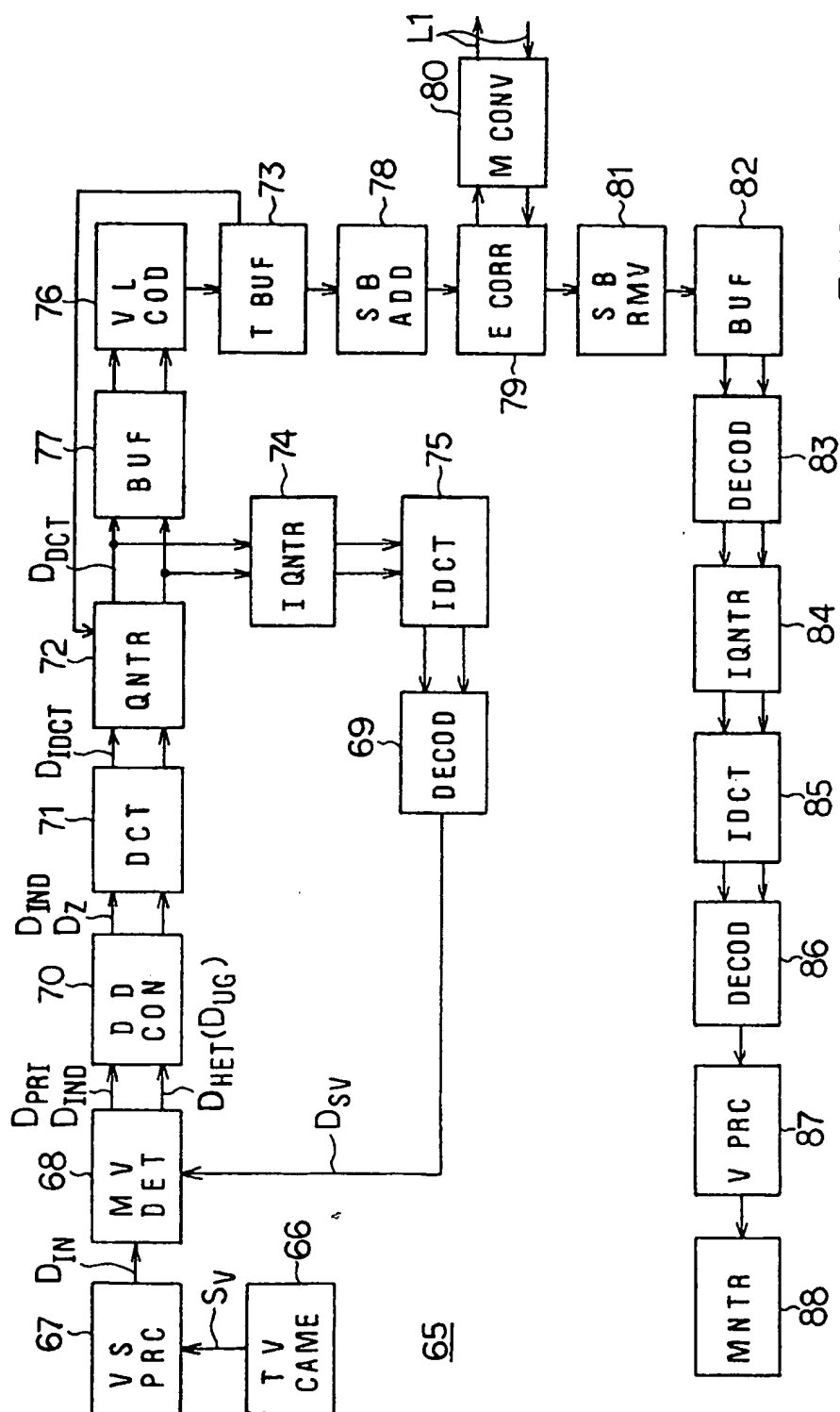


FIG.14



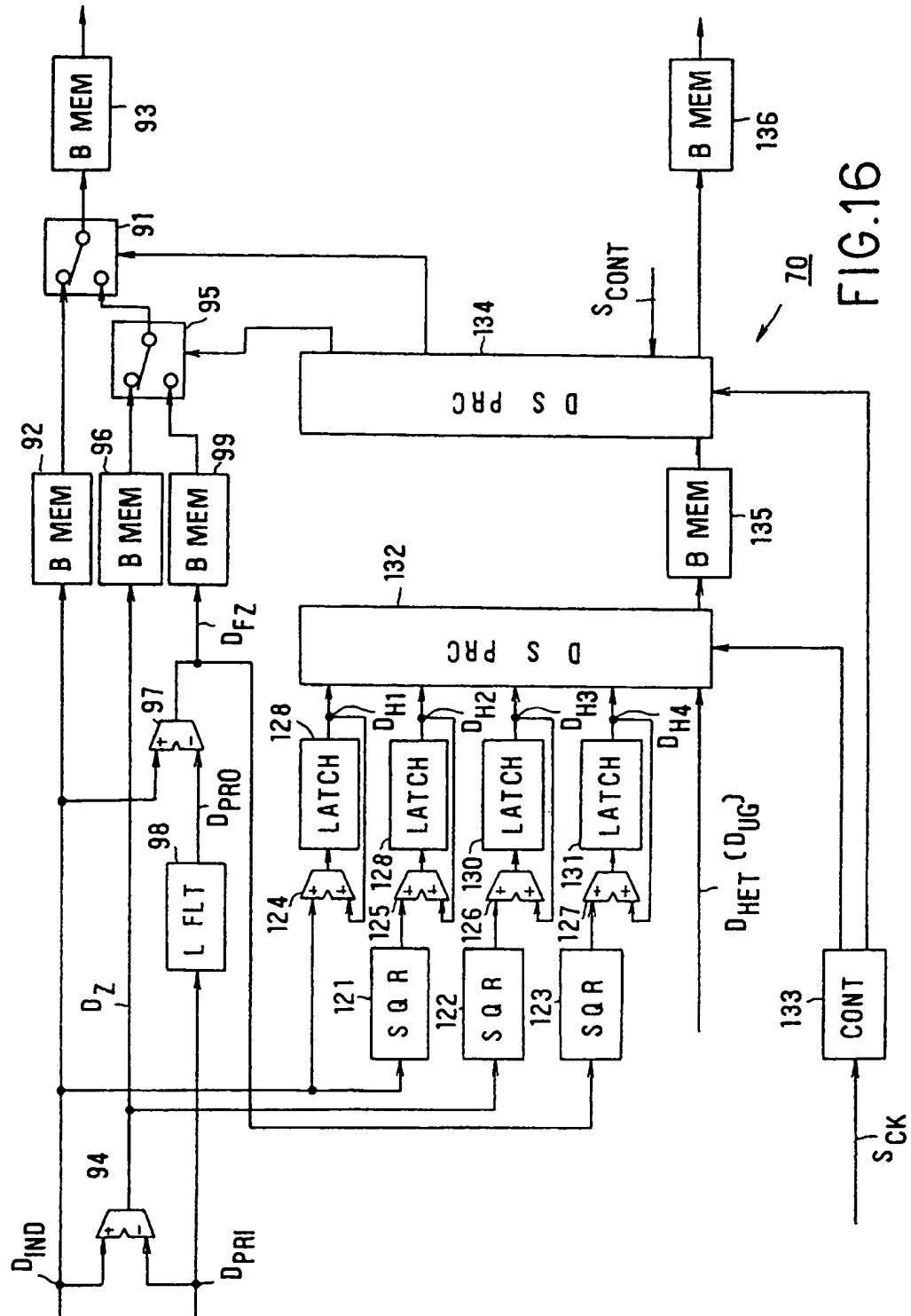


FIG.16

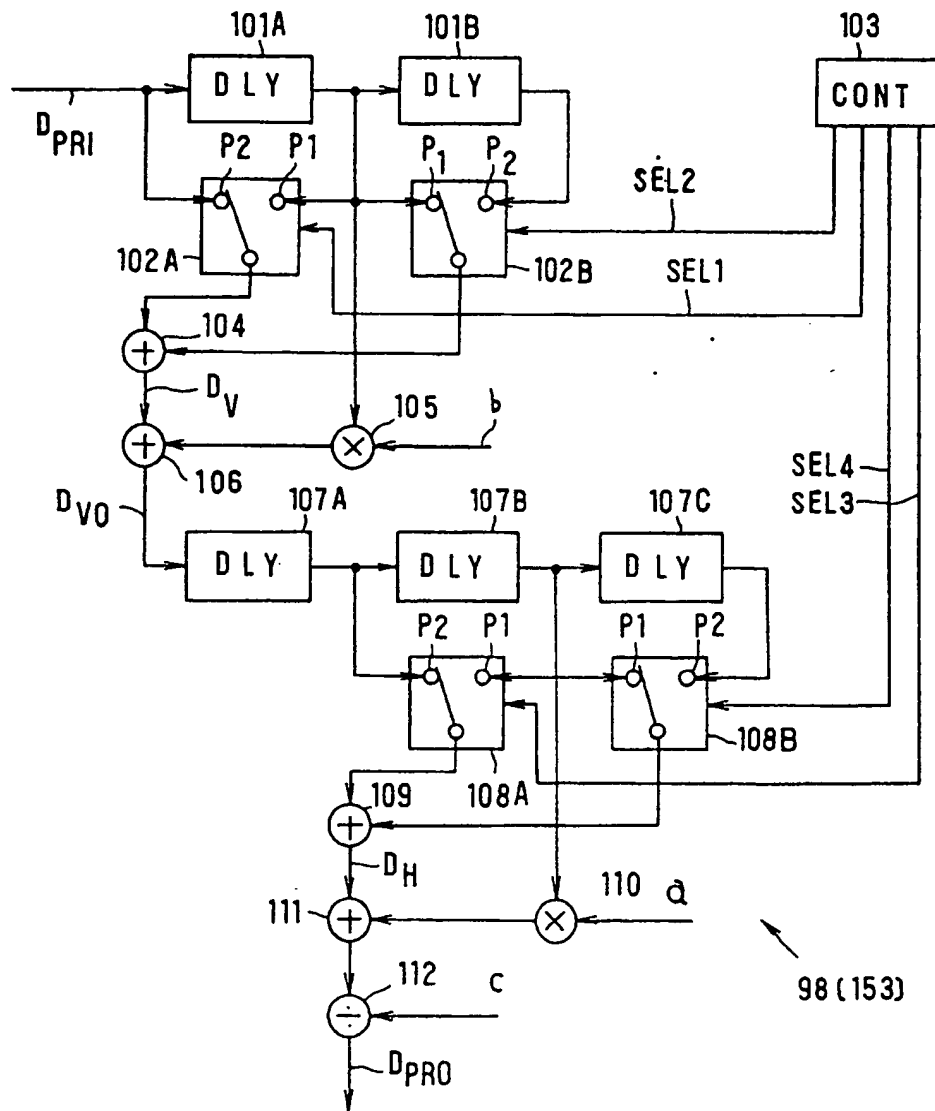


FIG.17

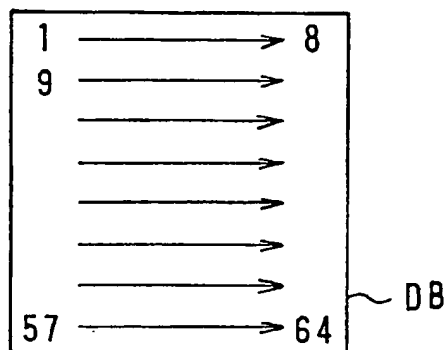


FIG. 18

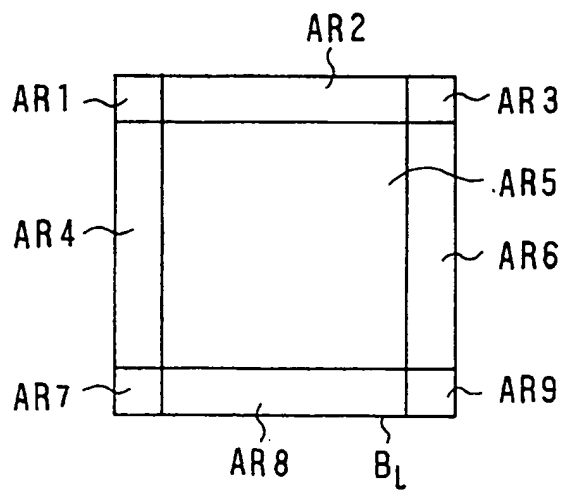


FIG. 19

	102A	102B	108A	108B	D _V	D _{VD}	D _H	D _{VD}
AR1	P1	P1	P1	P1	$2A_{0,0}$	$4A_{0,0}$	$8A_{0,0}$	$16A_{0,0}$
AR2	P1	P1	P2	P2	$2A_{0,0}$	$4A_{0,0}$	$4A_{-1,0} + 4A_{1,0}$	$4A_{-1,0} + 8A_{0,0} + 4A_{1,0}$
AR3	P1	P1	P1	P1	$2A_{0,0}$	$4A_{0,0}$	$8A_{0,0}$	$16A_{0,0}$
AR4	P2	P2	P1	P1	$A_{0,-1} - A_{0,1}$	$A_{0,-1} - 2A_{0,0} - A_{0,1}$	$2A_{0,-1} - 4A_{0,0} - 2A_{0,1}$	$4A_{0,-1} + 8A_{0,0} + 4A_{0,1}$
AR5	P2	P2	P2	P2	$A_{0,-1} + A_{0,1}$	$A_{0,-1} + 2A_{0,0} + A_{0,1}$	$A_{-1,-1} + 2A_{-1,0} + A_{-1,1} + A_{1,-1} + 2A_{1,0} + A_{1,1}$	$A_{-1,-1} + 2A_{-1,0} + A_{-1,1} + 2A_{0,-1} + 4A_{0,0} + 2A_{0,1} + A_{1,-1} + 2A_{1,0} + A_{1,1}$
AR6	P2	P2	P1	P1	$A_{0,-1} + A_{0,1}$	$A_{0,-1} + 2A_{0,0} + A_{0,1}$	$2A_{0,-1} + 4A_{0,0} + 2A_{0,1}$	$4A_{0,-1} + 8A_{0,0} + 4A_{0,1}$
AR7	P1	P1	P1	P1	$2A_{0,0}$	$4A_{0,0}$	$8A_{0,0}$	$16A_{0,0}$
AR8	P1	P1	P2	P2	$2A_{0,0}$	$4A_{0,0}$	$4A_{-1,0} + 4A_{1,0}$	$4A_{-1,0} + 8A_{0,0} + 4A_{1,0}$
AR9	P1	P1	P1	P1	$2A_{0,0}$	$4A_{0,0}$	$8A_{0,0}$	$16A_{0,0}$

FIG. 20

$A_{1,1}$	$A_{0,1}$	$A_{-1,1}$
$A_{1,0}$	$A_{0,0}$	$A_{-1,0}$
$A_{1,-1}$	$A_{0,-1}$	$A_{-1,-1}$

FIG. 21

	102A	102B	108A	108B
AR1	P1	P2	P1	P2
AR2	P1	P2	P2	P2
AR3	P1	P2	P2	P1
AR4	P2	P2	P1	P2
AR5	P2	P2	P2	P2
AR6	P1	P1	P1	P2
AR7	P1	P2	P2	P1
AR8	P1	P2	P1	P1
AR9	P1	P2	P1	P2

FIG. 25

000	000	000	000	000	000	000	000
010	121	121	121	121	121	121	010
000	000	000	000	000	000	000	000
010	121	121	121	121	121	121	010
020	242	242	242	242	242	242	020
010	121	121	121	121	121	121	010
010	121	121	121	121	121	121	010
020	242	242	242	242	242	242	020
010	121	121	121	121	121	121	010
010	121	121	121	121	121	121	010
020	242	242	242	242	242	242	020
010	121	121	121	121	121	121	010
010	121	121	121	121	121	121	010
020	242	242	242	242	242	242	020
010	121	121	121	121	121	121	010
010	121	121	121	121	121	121	010
020	242	242	242	242	242	242	020
010	121	121	121	121	121	121	010
000	000	000	000	000	000	000	000
010	121	121	121	121	121	121	010
000	000	000	000	000	000	000	000

FIG. 22

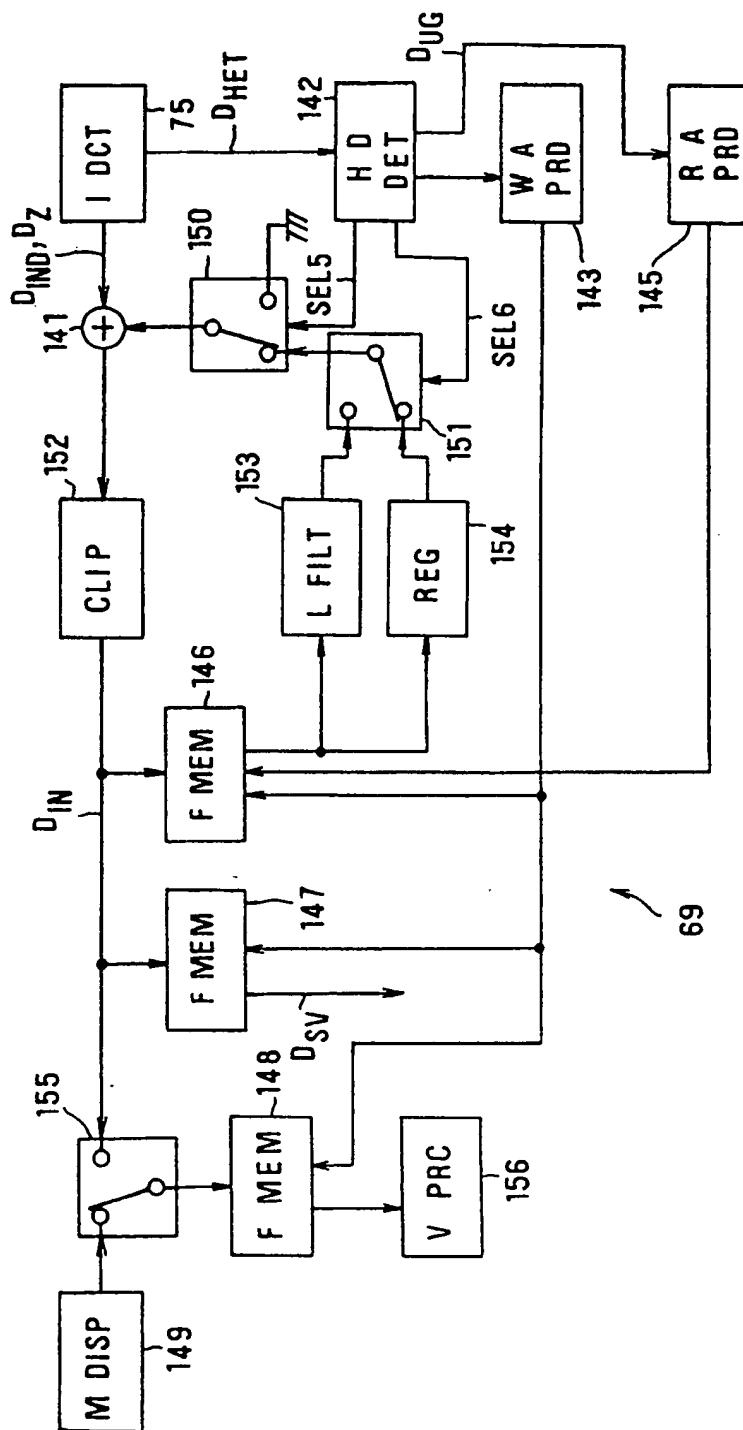
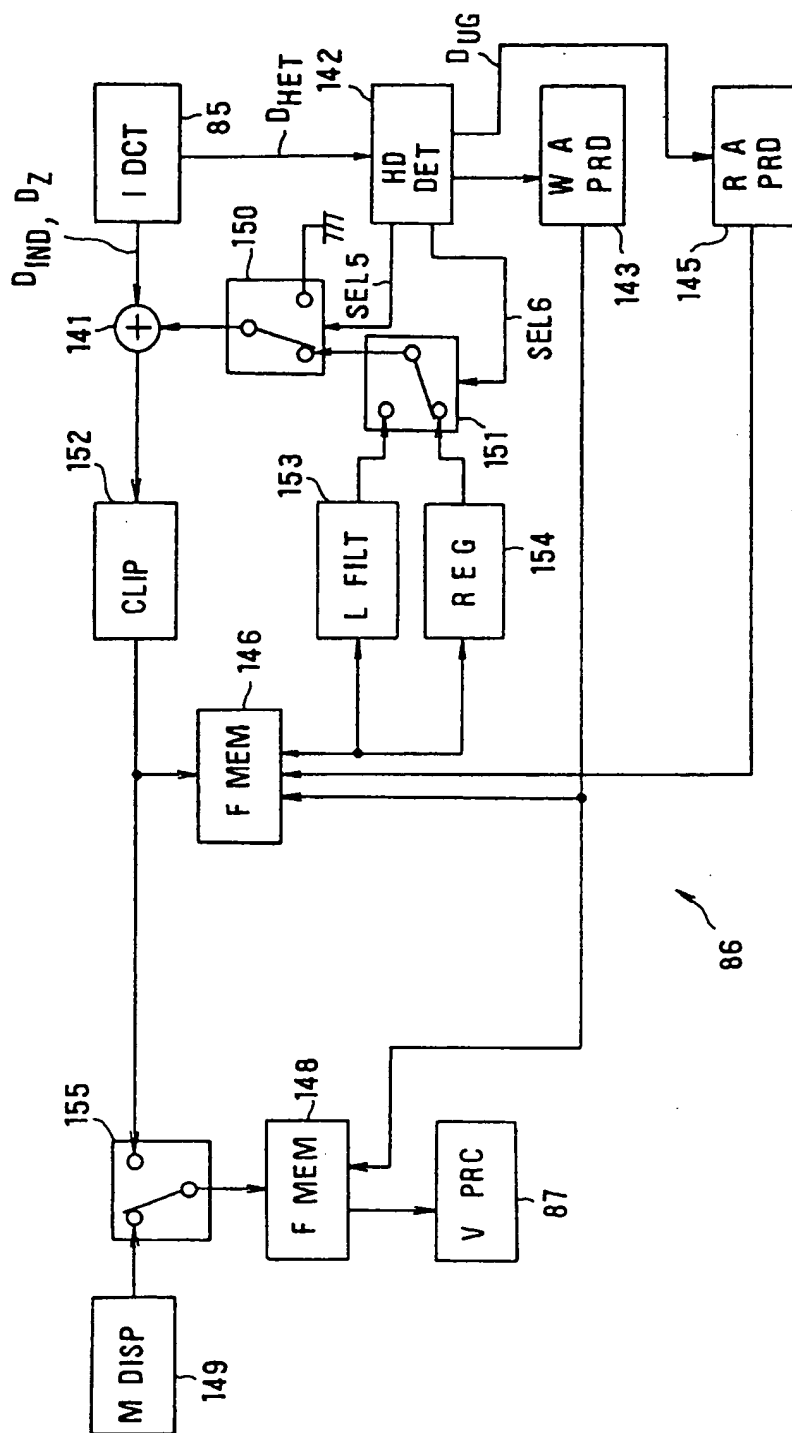


FIG. 23



000	000	000	000	000	000	000	000
093	363	363	363	363	363	363	093
031	121	121	121	121	121	121	130
031	121	121	121	121	121	121	130
062	242	242	242	242	242	242	260
031	121	121	121	121	121	121	130
031	121	121	121	121	121	121	130
062	242	242	242	242	242	242	260
031	121	121	121	121	121	121	130
031	121	121	121	121	121	121	130
062	242	242	242	242	242	242	260
031	121	121	121	121	121	121	130
031	121	121	121	121	121	121	130
062	242	242	242	242	242	242	260
031	121	121	121	121	121	121	130
031	121	121	121	121	121	121	130
062	242	242	242	242	242	242	260
031	121	121	121	121	121	121	130
000	000	000	000	000	000	000	000
093	363	363	363	363	363	363	093
031	121	121	121	121	121	121	130

FIG. 26

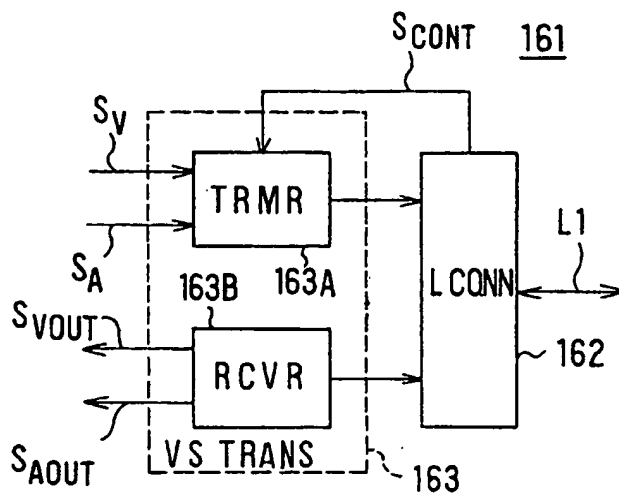


FIG.27

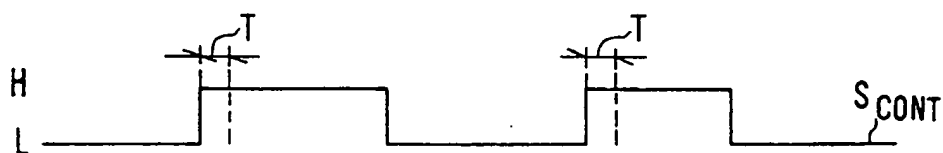


FIG.28